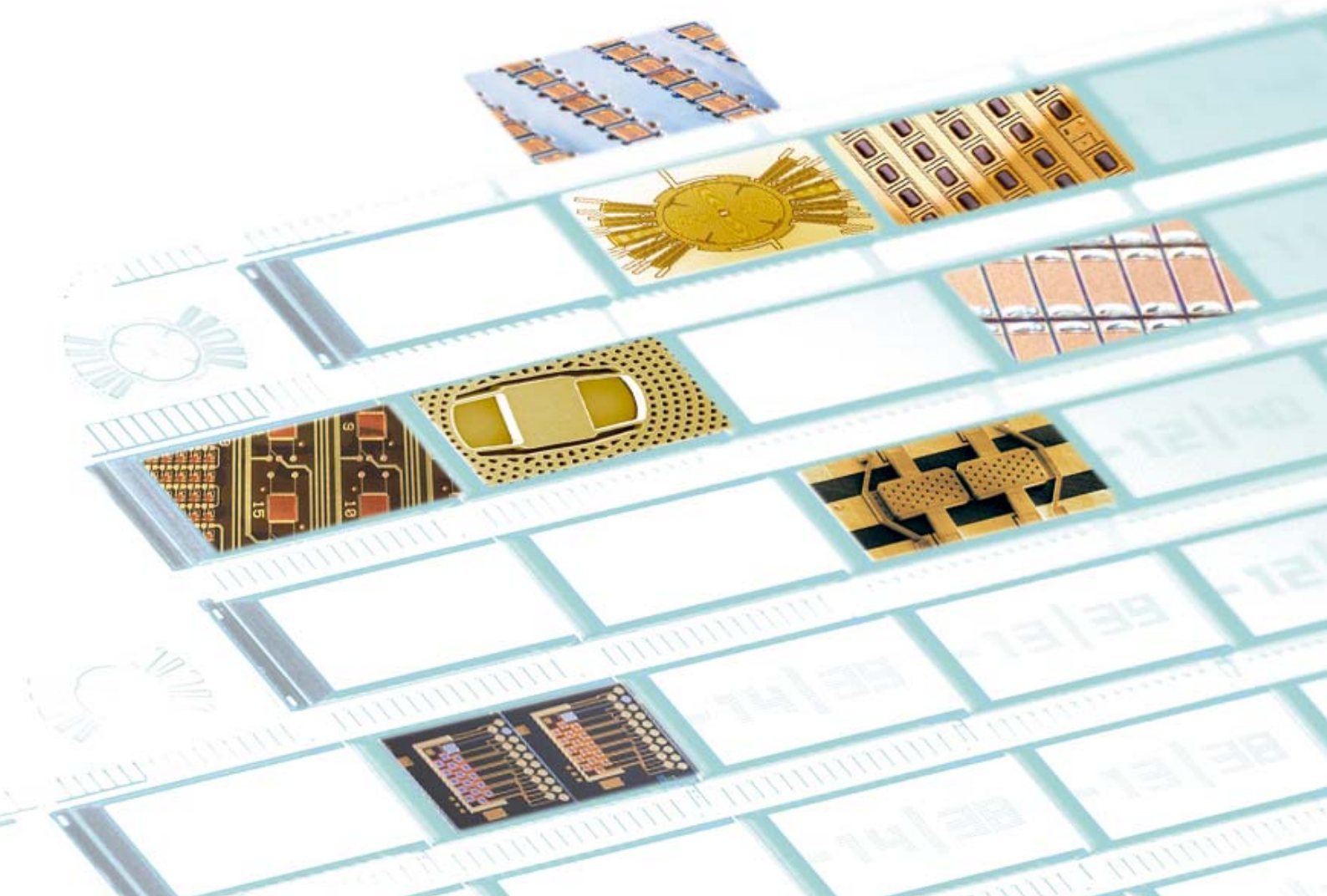
ISIT

Fraunhofer Institut Siliziumtechnologie

Achievements and Results
Annual Report 2005



Achievements and Results
Annual Report 2005

Waiting for the
Federal President at
Fraunhofer ISIT.

Achievements and Results
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Federal President Horst Köhler
and his wife Eva Luise Köhler; right:
Minister-President of Land Schleswig-Holstein
Peter Harry Carstensen.

From left to right: Prof. Anton Heuberger,
Minister of Science, Economic Affairs and
Transportation of Land Schleswig-Holstein
Dietrich Austermann, Dr. Rainer Hintsche.

Preface

Fraunhofer ISIT received a visit by German President Horst Köhler on Wednesday, May 25, 2005. His visit was undoubtedly the most prominent event of the year, and it was a great honor for the Institute and all of its staff.
The reason for this visit was to meet the winners of the German Future Prize 2004 – Dr. Rainer Hintsche, who works for the ISIT, Dr. Walter Gumbrecht from Siemens and Dr. Roland Thewes from Infineon. They had been jointly awarded the German President's prize for technology and innovation, probably the most prestigious award of this type in Germany, for their work on the development of electric biochip technology.

The German President was accompanied by the Prime Minister of Schleswig-Holstein, Peter Harry Carstensen, the Schleswig-Holstein economics minister, Dietrich Austermann, and Dr. Manfred Dietrich of the Federal Ministry of Education and Research BMBF.

The German President and his fellow visitors were brought up to date on the status of the project to scale up the prize-winning research work on electric biochip technology for industrial application, which has made considerable progress over the past year. Receiving the German Future Prize has not only greatly boosted the motivation of all concerned persons but also helped to launch many new aspects of the project in recent months and to advance them more rapidly. The effect of this outstanding distinction can also be discerned in the number and quality of offers of collaboration that the project team has been able to accept. It has been possible to embark on a variety of projects in different fields of application with industrial partners who possess specialized know-how on the user side. ISIT and its spin-off company eBiochip Systems GmbH are currently managing around 20 projects that cover a significant proportion of the huge range of potential applications for electric biochips. Such chips, configured to form a miniature 'lab-on-chip', are ideal for many types of analysis employed in environmental engineering, the food processing industry, and medicine.

Fraunhofer ISIT has successfully established its industrial-scale production line for silicon biosensor chips ranging from low-density devices to chips with 16 parallel test points and separate electronics, and developed its techniques for coating these chips with biological detection molecules to a mature, durably stable process. The spin-off company eBiochip Systems GmbH was formed by the Institute to market these products. The company's portfolio meanwhile features several types of fully automated portable analysis devices for the detection of proteins, nucleic acids and antibiotics, for example. Its electric biochip platform is being employed in numerous applications as part of a pan-European cooperation network comprising 15 partners in industry and science.

The company envisages significant results from its strategic alliance with DIEHL BGT Defense in the field of homeland security. This partnership has enabled eBiochip to market a product for the detection of biological warfare agents that has no competitors at the moment. It is the only portable measuring instrument capable of detecting and identifying biological weapons used in warfare and terrorism that are classified as toxins as well as those belonging to the categories of bacteria and viruses. The first lasting for months trial of these portable detection systems has been successfully completed by the German army, and ISIT is justifiably optimistic that these measuring systems will also be incorporated in the next

Assistant Head of Government Department Dr. Manfred Dietrich in discussion with Minister Dietrich Austermann.

generation of the "Spür-Fuchs" – armored vehicle to detect ABC-weapons – produced by Rheinmetall.

In December, the Institute's electric biochip technology received another major international accolade. Rainer Hintsche was awarded the European Grand Prix of Innivation in Monaco for his analysis device for the detection of biological warfare agents. This highly regarded European prize for applied research and technology development was awarded for the twelfth time in 2005, with a focus on security technologies in that year's competition.

The outstanding results that the ISIT is now achieving with its electric biochip technology were unimaginable when the first development projects were started in 1990. It took almost 10 years to establish the basis for the technology. The ISIT invested around 5 million Euros of its own financial resources, largely set aside from other sources of funding. The breakthrough came when I succeeded in convincing Dr. Dietrich at the BMBF of the advantages of electric biochips. With Dr. Dietrich's help, we were able to launch the lead project "Sibanat" with project funding of 10 million Euros. I would like to take this opportunity to extend my sincere thanks to Dr. Dietrich once again for his extraordinary effort and support.

Federal President Horst Köhler visits the ISIT cleanroom.

In addition to Rainer Hintsche, two other members of ISIT staff received distinctions. One was Dr. Wilhelm Brünger, who was awarded for his many years of scientific work in the field of electron-beam lithography at the international MNE conference in Vienna in September. The other was Ragna Berenike Rühe, who completed her education as a microtechnologist at ISIT with the best marks in the country. The prize awarded to Ragna Rühe is all the more gratifying for ISIT in that it demonstrates the uniquely excellent spirit of cooperation that has developed between our trainees and the microtechnology training staff at ISIT, at Vishay and the teachers at the vocational school in Itzehoe over the past years.

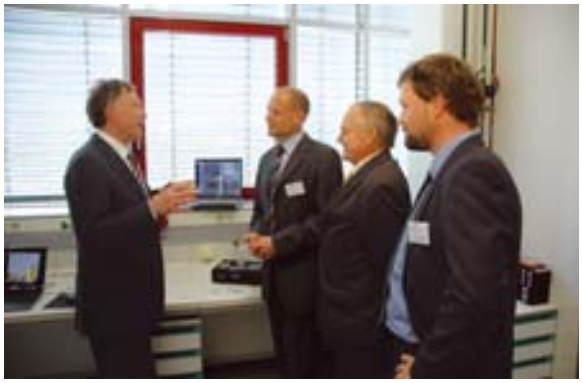
The high-tech community in Itzehoe suffered a grievous loss in the late summer. Dr. Ingo Hussla, the managing director of the IZET innovation center in Itzehoe, died on September 19 at the age of only 57 years, following a short, serious illness. Dr. Hussla was one of the most faithful proponents of Itzehoe's qualities for a high-tech location. Ingo Hussla played a major role in attracting numerous small and large companies to choose a location in Itzehoe, thus creating a great number of sustainable jobs. It is certainly thanks to his efforts that Itzehoe has become a crystallization point for high-tech firms. Ingo Hussla fought untiringly to support the high-tech community in Itzehoe. He was a lively, creative person who never stood still. He

developed and implemented innumerable ideas, founded dozens of initiatives, and was altogether an inspiring force through his unshakably optimistic spirit of an entrepreneur. His job was to promote the region's capacity for technological innovation and encourage new firms to settle here. Dr. Ingo Hussla took care on this task with an astonishing degree of commitment, and went on to make it his life's work. His untiring efforts have spread the name of Itzehoe national and international as a synonym for high technology.

As in previous years, ISIT has progressed with its plans to modernize and extend the facilities available at the Institute. This year, the research and development laboratories and production line for microelectronic and micromechanical components was modernized and re-equipped with the support of the state government. From now on, companies working in Itzehoe will be able to handle silicon wafers with a diameter of 200 millimeters instead of substrates based on the former standard of 150 millimeters. The larger-diameter wafers represent a pioneering

From left to right: ISIT-IC Designer Oliver Schwarzelbach, Prof. Anton Heuberger, Minister Dietrich Austermann.

Federal President Horst Köhler in conversation with the prizewinners Dr. Walter Gumbrecht, Dr. Rainer Hintsche and Dr. Roland Thewes.

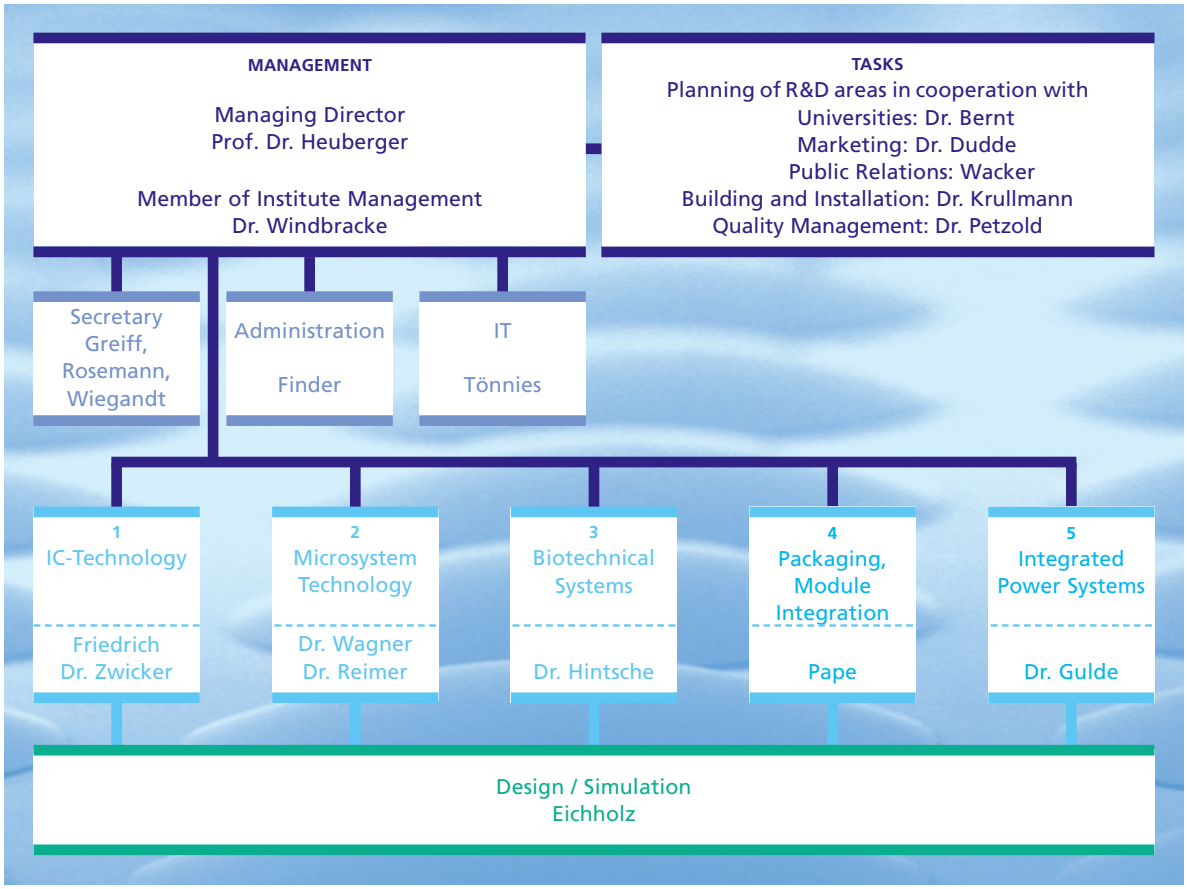


ISIT scientist Dr. Eric Nebling presents technological details.

ISIT scientist Dr. Thomas Ahrens (right) inaugurates the new training line for lead-free electronic production.

work, given that nowhere else in the world has a 200-millimeter semiconductor production line for the manufacture of microsystems. Retooling for the new wafer size has involved an enormous development challenge. Without the support of the state government, ISIT would not have been able to accomplish the necessary technological development work. For this reason, I would like to thank the new state government for the excellent collaboration, and most particularly the new economics minister Dietrich Austermann, who has consistently stood by my side for many years now. Thanks to this modernization work, the Institute in Itzehoe will be even better able to serve the industry as an attractive provider of research and development services. In this context, and on behalf of the ISIT, I would like to thank the director of Vishay, Dr. Paul, for his sustainable support.

ISIT has also brought forward this year its product-related research and development projects in an industrial environment. An example is the startup company SensorDynamics AG, whose close ties with the Institute have considerably advanced its status as a specialist in the integration of innovative sensor systems. The joint production capacity provided by SensorDynamics and the ISIT have made them one of the most productive suppliers of sophisticated, technically complex microsystems in Europe. ISIT and SensorDynamics are currently working together on the development of specific sensors (Gyros) for a major automotive supplier, one of the largest and most ambitious projects that the Institute has on its books for the coming years. These highly complex components detect the changes in direction of a solid mass in space. When incorporated in passenger vehicles, they can actively control driving dynamics or improve the accuracy of GPS coordinates. The sensor modules consist of a micromechanical sensor and large-scale-integrated system electronics. Presently the partners are preparing for industrial series production.
As things stand today a production demand by the automotive sector of roughly 10 million sensors per year between now and 2010 is anticipated.



ISIT Organigram

In the year under review, another new service for the industry was created in Itzehoe. The ISIT has set up a technology and competence center for lead-free manufacturing of electronic circuits in Itzehoe, including a specific production line for training. The impulse for setting up this production line comes from an EU directive which stipulates that, with a few special exceptions, all electronic assemblies brought onto the market after July 2006 must be lead-free. This represents a fundamental break in tradition for the entire electronics industry. Many manufacturing firms will be obliged to come to terms with major technical challenges, given that adapting to new processes for lead-free soldering involves working with much higher processing temperatures. The Institute's new center enables companies to test their new lead-free manufacturing processes and train their employees without any loss in productivity.

The examples cited above show that 2005 was a highly successful year for the ISIT. These results are largely due to the dedicated work of the Institute's highly qualified teams of researchers and their cooperation partners. I would therefore like to extend my heartfelt thanks to all members of staff in Itzehoe.

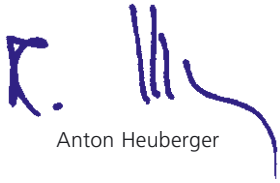
Let me conclude by adding a few comments concerning the hotly debated topics of microtechnology and nanotechnology, which are currently being discussed in policy-making circles. Over the last twenty years, technological

High Tech Itzehoe: SMI (red building), Fraunhofer ISIT and Vishay Siliconix Itzehoe (largest complex) Bullith Batteries and Condias (bottom), IZET Innovationszentrum (right), Nippon Antenna (white round building) and Procon (upper right).

Member of board of the Fraunhofer-Gesellschaft Dennis Tsichritzis congratulates Ragna Berenike Rühe to her excellent examination.

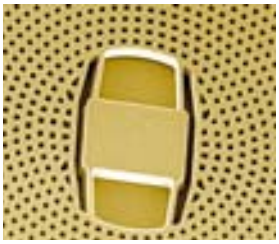
progress has been dominated by advances in the field of microelectronics. This has resulted in a technology for silicon-based electronic circuits whose dimensions extend to the sub-micrometer range, a technology that is now the basis for the upcoming technology leap into the area of complex microsystems.

In order to realize these ambitions, microengineering and microsystems technology have to be developed further in an effort to considerably improve their performance. Hence the prefix "nano" has been established in our everyday language. This is an understandable development, as "microsystems" and related terms date from the 1980s and are now beginning to sound old-fashioned. We need a new significant term that symbolizes technological progress. The problematic aspect of all these terms, apart from their lack of originality, is that they imply a fixed relationship with a specific scale of structural dimensions. In my view, the prefix "nano" not only stands for an even greater reduction in structural dimensions but also signifies a greater degree of system complexity and multifunctional attributes. Most microsystems these days are still based on microscale structures, yet microelectronics is already being pervaded by nanotechnology. The possibility of using structures well below 100 nm, in other words genuine nanostructures, is already being contemplated. It will certainly not take long before the first ultra-large-scale integrated electronic components based on design rules of 50 nm, for example, will hit the market. If one bears in mind that the main component of a microsystem is still the integrated circuit, but with structures now being on the nanoscale, the term "nanotechnology" is not so badly chosen after all. Silicon-based microelectronic circuits are likely to remain the only technical means of realizing the concept of artificial intelligence for a long time to come.

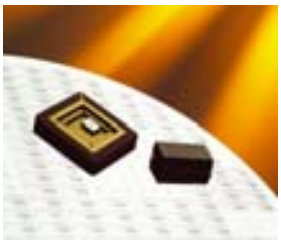


Anton Heuberger

Brief Portrait



Fraunhofer ISIT
Research and Production at one Location



Gyro devices for automotive applications – a cooperation between SensorDynamics and Fraunhofer ISIT.

The Fraunhofer-Institut für Siliziumtechnologie (ISIT) develops and manufactures components in microelectronics and microsystems technology, from the design phase – including system simulation – to prototyping and fabrication of samples, up to series production. Though components such as valves and deflection mirrors manufactured by ISIT often measure just a fraction of a millimeter in size, their range of applicability is anything but small: the devices are implemented in areas as diverse as medicine, environmental and traffic engineering, communication systems, automotive industry, and mechanical engineering. Working under contract, ISIT develops these types of components in accordance with customer requirements, also creating the application-specific integrated circuits (ASICs) needed for the operation of sensors and actuators. Included in this service is the integration into the overall microsystem using miniaturized assembly and interconnection technology.

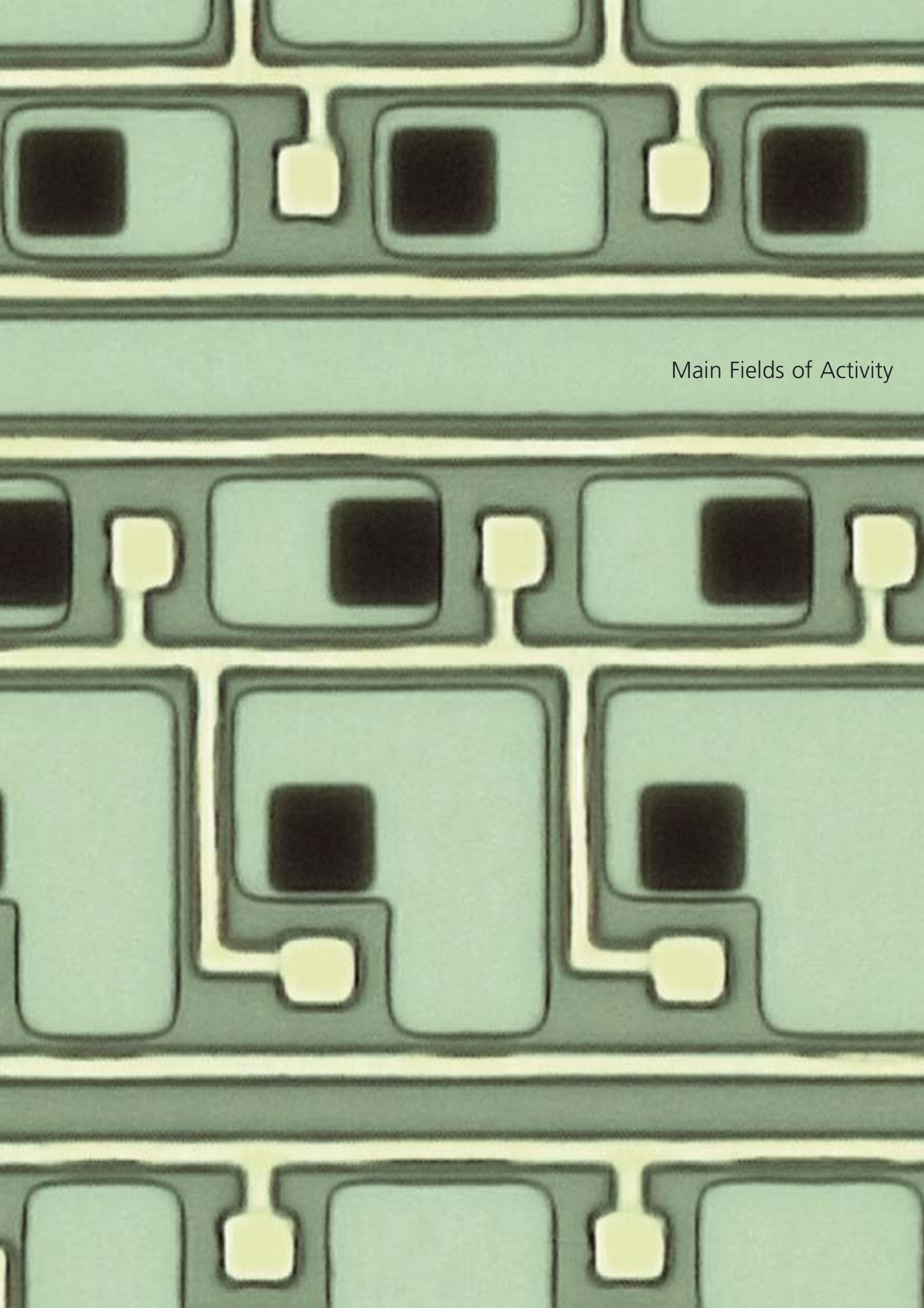
Together with Vishay Siliconix Itzehoe GmbH, the institute operates a professional semiconductor production line which is up-to-date in all required quality certifications. The line is used not only for producing microelectronic components (PowerMOS) and microsystems, but also for R&D projects aimed at developing new components and technological processes. An ISO-9001-certified quality management system serves as the basis for the development, qualification and production of micro-engineered components.

Other groups at ISIT carry out work on assembly and packaging techniques for microsystems and sensors, analyze the quality and reliability of electronic components, and develop advanced power-supply components for electronic systems.

The institute employs a staff of around 150.

Check for solder heat resistance of SMD components in the ISIT lead-free training line.

Tunable capacitor.



Main Fields of Activity

Microsystems Technology (MEMS) and IC Design

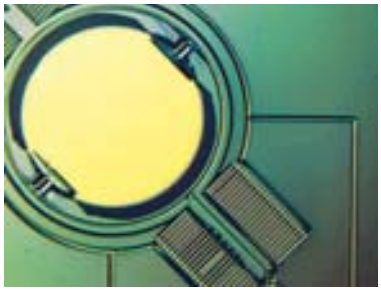
The work performed at the institute focuses predominantly on microsystems technology, an area which ISIT has pioneered in Germany. For over 20 years ISIT scientists have been working on the development of micromechanical sensors and actuators, micro-optic, and components for radio-frequency applications (RF-MEMS). Their work in this area also includes integrating these components with microelectronics to create small-size systems of high functionality. A multitude of components and systems have originated at ISIT.

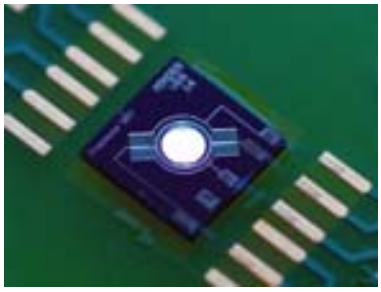
The current emphasis in the area of sensor technology is on inertial sensor technology (acceleration, angular rate, inertial measurement units), pressure, and flow sensors, all with integrated electronics (ASICs). A microsensor core technology using thick polysilicon structural layers and waferlevel hermetic sealing is available.

The development of customized integration concepts, ranging from simple, cost-effective assembly in a common package to complete monolithic integration, represents the core of ISIT's offerings in this area. One integration technique that customers may find particularly valuable is the ability to mount a microsystem on the surface of a fully processed ASIC wafer using a low-temperature process such as electroplating.

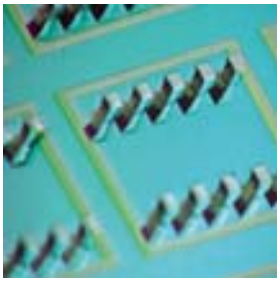
ISIT also develops optical microsystems, primarily for optical instrumentation, consumer products and communication. Examples include micro-mirrors for laser projection displays, laser scanners and analog or digital light modulators, and passive optical elements such as refractive and diffractive lenses, prisms, or aperture systems. Radio-frequency microsystems developed at ISIT, designed primarily for use in reconfigurable wireless communication devices, include RF-MEMS switches, tunable capacitors, and ohmic switches.

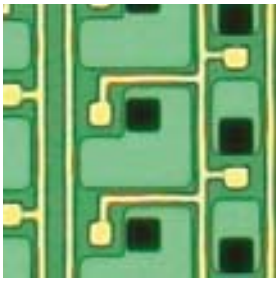
Among the key fluidic components created at Fraunhofer ISIT are pneumatic valves, bi-stable fluid valves, sensor-controlled automatic microdosing devices, and micropumps, all of which can also be employed in Lab-on-Chip systems.





Two axis micro mirror developed for laser projection applications.





Electrical feedthrough patterns (left).

Detail of an electron beam aperture plate (right).

On-chip integrated microactuator systems are especially challenging in order to meet the specific requirements in the micro- and nanometer scale. In this field ISIT has a high expertise and implements electrostatic, thermal and — more recently — high-speed high-force piezoelectric actuation principles on silicon wafers.

The service approach enables ISIT to offer its customers all of these components as prototypes and also to manufacture them in series according to the customer's specific needs, utilizing the quality and capacity of the institute's in-house semiconductor and MEMS production line. The services provided also include application-specific microsystem packaging at wafer level, including thin wafer and vertical feedtrough capabilities.

Should a customer's requirements fall outside the scope of the institute's technological capabilities, ISIT can utilize an European network to gain access to other manufacturers and processes, like production lines at Bosch, SensoNor, HL Planar, ST and Tronic's. ISIT organizes the production as a foundry service for interested customers. And with the settlement of SMI GmbH in Itzehoe, the institute has gained a key partner for producing microsystems and related components as a foundry service under customer contract.

One of the prerequisites for developing original microsystems and microelectronic components is a highly capable circuit design group. The staff at ISIT are specialists in the design of analog/digital circuits, which enable the electronic analysis of signals from silicon sensors. The designers at ISIT also model micromechanical and micro optic elements and test their functionality in advance using FEM and behavorial modeling simulation tools.

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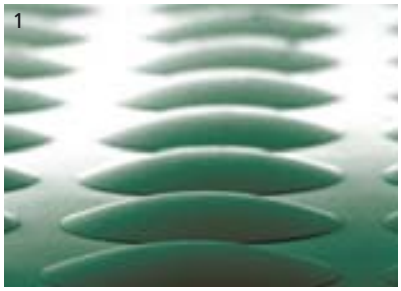
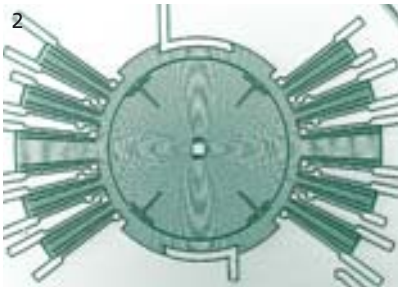
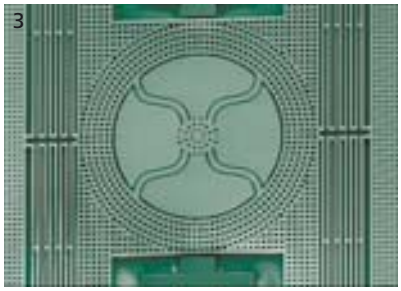
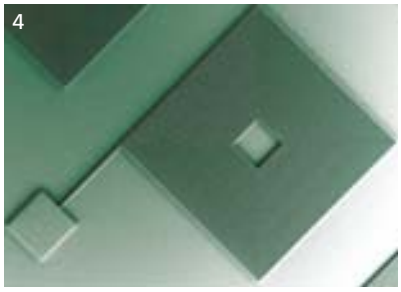
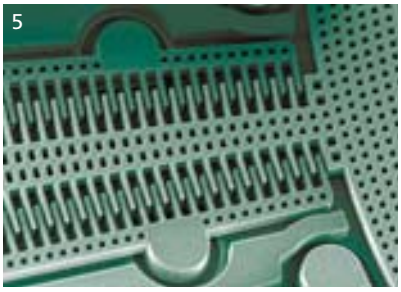










Specific MEMS structures:
1 Optical micro lenses.
2 Gyroscope.
3 Magnetometer.
4 Microcoil.
5 Detail of gyroscope

IC Technology and Power Electronics

The power electronics and integrated circuits group develops and manufactures active integrated circuits as well as discrete passive components. Among the active components the main concern lies on power devices such as smart power chips, IGBTs, bi-directional components, PowerMOS circuits and diodes. Thereby ISIT primarily uses Vishay's customized, individual production sequences. Additional support for work in this area is provided by an array of modified tools for simulation, design and testing. The ISIT also benefits from years of experience in the design and construction of CMOS circuits.

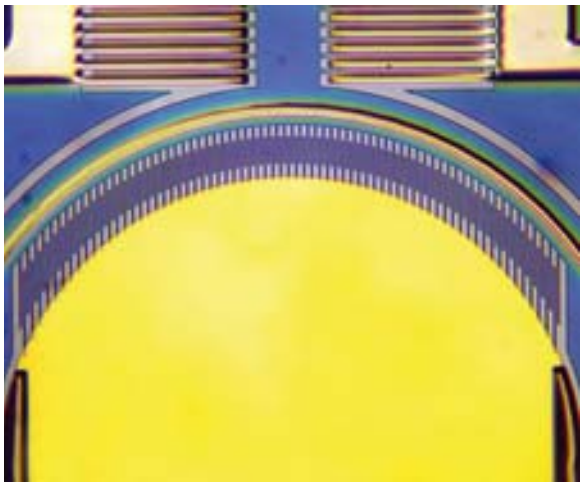
The passive components developed and fabricated at ISIT are primarily chip capacitors, precision resistors and inductors. Materials development and the integration of new materials and alloys into existing manufacturing processes play an important role in the development process.

ISIT develops individual processes, process modules and complete process flows for diverse applications. The institute also offers customer-specific silicon components processing in small to medium-sized batches on the basis of a qualified semiconductor process technology.

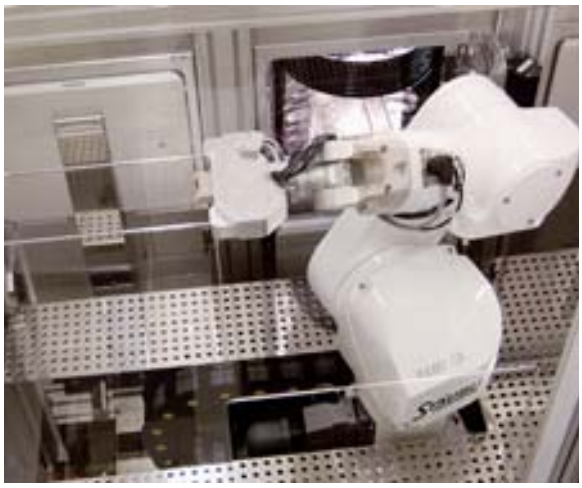
To support the development of new semiconductor production techniques, production equipment of particular interest is selected for testing and optimization by the ISIT staff. This practice provides the institute with specialized expertise in challenges related to etching, deposition, lithography, and planarization methods. Planarization using chemical-mechanical polishing (CMP) in particular is a key technology for manufacturing advanced integrated circuits and microsystems.

The intensive work done by ISIT in this area is supported by a corresponding infrastructure: The institute's CMP application lab is equipped with CMP cluster tools, single- and double-sided polishers and post-CMP cleaning equipment for wafers with 100 to 300 mm in diameter. The CMP group at ISIT works in close relationship to Peter Wolters Surface Technologies GmbH since many years, as well as other semiconductor fabrication equipment manufacturers, producers of consumables, CMP users and chip and wafer manufacturers.

In future micro mirror fabrication requires CMP technology for extreme smooth surfaces.



Handling robot of Peter Wolters HFP™ CMP cluster tool.



Peter Wolters PM 200 CMP™ cluster tool for planarization of MEMS devices.

The group's work encompasses the following areas:

- Testing of CMP systems and CMP cleaning equipment
- Development of CMP processes for
  - Dielectrics (SiO_2, TEOS, BPSG, low-k, etc.)
  - Metals (W, Cu, Ni, etc.)
  - Silicon (wafers, poly-Si)
- Testing of slurries and pads for CMP
- Post-CMP cleaning
- CMP-related metrology
- Implementation of customer-specific polishing processes for ICs and microsystems

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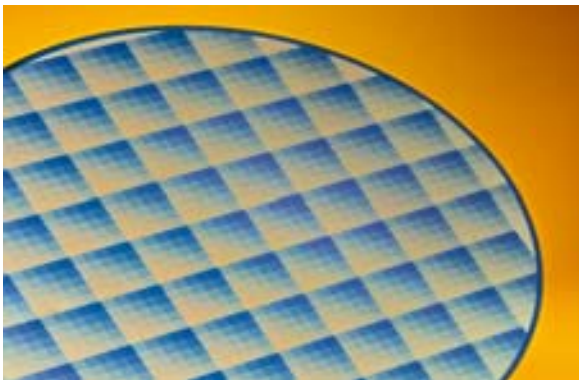
Wafer transfer station of Peter Wolters HFP™ CMP cluster tool.



200 mm CMP test wafer.

Biotechnical Microsystems

ISIT is worldwide leading in electrical biochip technology, and is holding around 20 patents in the area. The electrical biochips offer the intrinsic advantages vs. optical biochips because of direct miniaturization and transmission of responses of biochemical reactions into computing networks. Employing new nm-ultramicroelectrodes and integrated reference and auxiliary electrodes the construction enables powerful sensor micro arrays and the use of ultra-sensitive, ultra-selective measurement techniques, such as "redox recycling". In combination with microfluidic components and integrated electronics, these electrical micro arrays represent the fastest and most cost-effective basis for mobile analysis systems, which can be used to identify and quantify DNA, RNA, proteins and haptens.

Those electrical micro arrays, which are wireless packaged into proprietary "Chip-Sticks" are useful to detect a variety of analytes simultaneously. ISIT works closely with the Itzehoe based company eBiochip Systems GmbH (www.ebiochip.com), an ISIT spin-off, to facilitate the marketing of these new technologies. eBiochip Systems developed a variety of smart and portable instruments, from a low end device for education and demonstration to the high end fully automated micro array analyzer. Demonstrating very competititve applications as the identification and quantification of protein and pathogenic biowarfare agents or the antibiotics in raw milk the platform of electrical biochip technology is successfully used in several labs in Europe and in EU granted projects.

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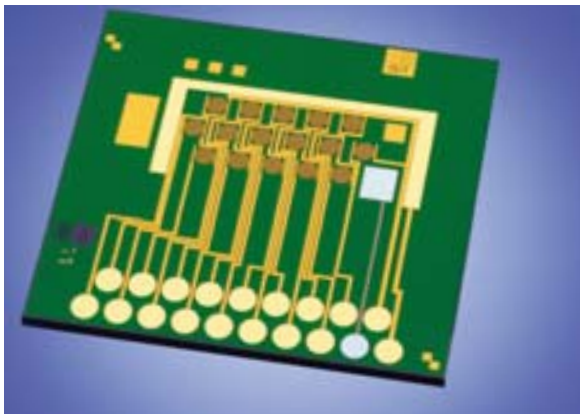
Different automated eBiochip measuring systems to detect biological agents.



Electrical Silicon biochip with integrated reference electrode.

Dispensing bio molecules on electrical biochips in cleanroom environment.

Production tool for wafer level CSP manufacturing, developed at Frauhofer ISIT together with Wagenbrett GmbH.

Packaging Technology for Microelectronics and Microsystems

The assembly and interconnection technology group offers customers a broad range of services, including precision assembly of microstructured components and development and qualification of customer-specific packaging. Work in this area includes hermeticity and material compatibility tests for assemblies that have to work in aggressive environmental conditions, e.g., analysis of microsystem packages intended for in vivo use in medical technology.

Another focal area is miniaturization of chip and sensor assemblies and packages, which includes direct assembly of bare silicon chips. The institute possesses capabilities in all of the essential technical stages for chip-on-board (COB) technology, from designing the circuit boards to qualified COB assemblies. The bare ICs and microsensors are mounted using the Chip & Wire or Flip-Chip techniques.

The group also develops processes for assembling and packaging chips and sensors/actuators while still on the wafer. Due to the increasing global trend among chip manufacturers to implement this special packaging process, Wafer Level Packaging (WLP) – now considered the assembly technique of the future – has become a central focus of the group's work. WLP technology can also be applied for packaging sensors under vacuum, such as angular rate or acceleration sensors. ISIT has successfully integrated thin film getter layers for high-Q microresonators and improved vacuum lifetime.

The institute is active in this area not only as a technology developer, but also as a manufacturer of assemblies for its customers using the available Chip-Size-Packaging production line.

The group also develops ultra-thin electronic assemblies, which involves stacked mounting flexible silicon chips as thin as 50 µm on flexible substrates. These techniques will ultimately lead to further miniaturization in existing systems, such as laptops, hand held PCs or mobile phones, but will also enable the development of new products like intelligent flexible product labels or smart clothes.

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Card with three apertures for UV-laser ablation of the cornea of human eyes; small picture: detail.

Cap wafer with individual getters for high vacuum sensor encapsulation on wafer level.

Quality and Reliability of Electronic Assemblies

Quality evaluation – in particular for the soldering work done in pre-production, pilot and main series lots – represents a continuous challenge for ISIT, for example whenever new technologies such as lead-free soldering are introduced, when increased error rates are discovered, or if the institute desires to achieve competitive advantages through continual product improvement.
To reveal potential weak points, ISIT employs both destructive and non-destructive analysis methods, such as x-ray transmission radiography and scanning acoustic microscopy. Working from a requirements matrix, ISIT scientists also evaluate long-term behavior of lead-free and lead-containing assemblies alike. They then formulate prognoses on the basis of model calculations, environmental and time-lapse load tests, and failure analysis.

In anticipation of a conversion to lead-free electronics manufacturing, Fraunhofer ISIT is undertaking design, material selection and process modification projects. To effect a further optimization of manufacturing processes, the institute applies process models and produces samples on industry-compatible equipment. The group also addresses issues related to thermal management and reliability for customer-specific power modules. In addition to these technological activities, the group regularly holds training sessions, including multi-day classes, at the institute or at company site.

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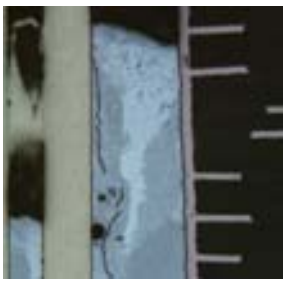
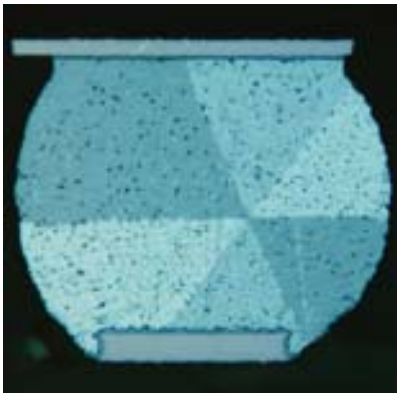
Optimizing RoHS compatible process in the lead-free training line.



Insufficient vertical fill: microsection polarized light contrast.



BGA ball: microsection polarized light contrast.

Lead-free "Wörthman" wave.

Integrated Power Systems

There is an ever increasing demand for high performance rechargeable batteries for mobile applications. Adequate battery solutions for mass products are available. Applications with special needs regarding electrical performance and design of the energy storage unit call for solutions which can not be provided by the standard battery products. A new lithium rechargeable battery design developed by ISIT over the last few years – for which the institute has applied for several patents -some are already granted- is capable of meeting these demands. This new concept, which features solid-state electrolytes, affords the same performance typical of Lithium-ion rechargeables, but it does not need the complicated rigid packaging technology required with conventional Lithium-ion batteries, which contain free liquid electrolytes. The battery package consists of a metallised heat-sealable plastic foil to make it air- and moisture-tight, resulting in a lower overall weight for the finished product.

ISIT's Lithium battery production process is based on the lamination of customized flexible foils containing the functional materials. This allows for tailor-made-battery solutions in a much greater variety of shapes and sizes, thus significantly diversifying the range of possible applications. Currently ISIT offers two systems characterised by different anode materials:

- The 3,7 V system is optimised with respect to power density
- The 2,3V system shows excellent robustness and long term stability

ISIT offers a variety of services: development, fabrication and small series production of customer-specific battery formats (ranging in size from micro-systems to laptops) in a broad range of available ampere-hour ratings, with various form factors and housing materials (e.g. plastic or Titanium). Following the preparation of samples, ISIT supports the customer in the transition to series production. The institute also provides application-specific material selection of various compounds for cathodes (e.g. Lithium Cobaltite, Lithium Iron Phosphate) and anodes (Graphite, Lithium Titanate, etc.) to ensure optimal conformity to the application requirements (e.g., power density, cycle stability, capacity, product life cycle, self-discharge rate...). Battery characterization and long-term electrical/environmental tests complete the range of services. In close cooperation with an industrial partner ISIT established an initial production line for an industrial-scale production process, which allows for a rapid ramp up of battery production.

Lithium polymer battery production in Itzehoe.

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Facilities and Equipment

In terms of both space and technical capabilities, the facilities at Fraunhofer ISIT provide an ideal environment for research & development work as well as production. In addition to its 150/200 mm (class 1) silicon technology line and 2500 m^2 of clean-room space, the institute has a further 450 m^2 of clean-room area (class 100) for specific microsystems engineering processes, including: wet-etching processes, high-rate plasma etching, deposition of non-IC-compatible materials, lithography with thick resist layers, gray-scale lithography, electroplating, microshaping and wafer bonding. Further 200 m^2 clean-room (class 100-1000) is equipped for chemical-mechanical polishing (CMP) and post-CMP cleaning. ISIT also offers a diverse selection of labs (1500 m^2) that are utilized by working groups for the development of chemical, biological and thermal processes, electrical and mechanical component characterization, and for assembly and interconnection technology. A spin-off arising from the work in assembly and interconnection technology – a CSP (Chip-Size Packaging) production line with an annual capacity of 100,000 wafers – was built in the ISIT clean rooms in collaboration with SMI GmbH (Silicon Manufacturing Itzehoe). The line is jointly operated by ISIT and SMI. The ISIT facility also operates a pilot production line for Lithium-polymer rechargeable batteries with power capacities of up to several ampere-hours.

Cleaning module of PM 200 CMP™ cluster tool for MEMS applications.

Offers for Research and Service

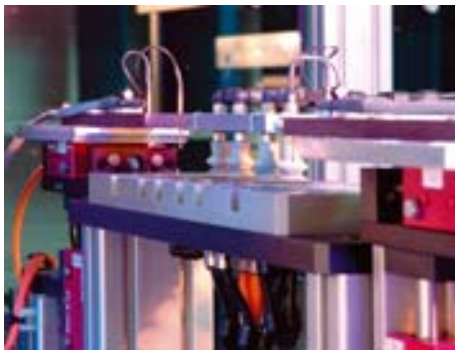
Assembly of Lithium polymer battery stacks.

Spectrum of Services

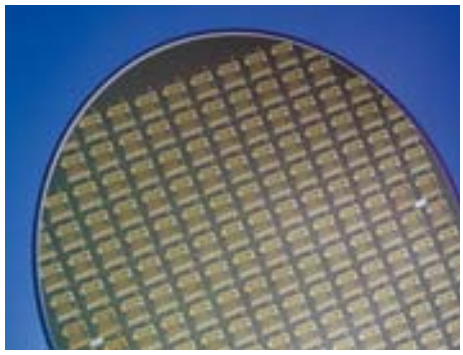
The institute makes its range of services available to companies representing a wide variety of branches, including medical technology, communication systems, automotive industry, and industrial electronics, just to name a few. After industrial customers specify necessary requirements of the components and systems, ISIT engineers work closely with them to design, simulate and produce the components, systems and manufacturing processes. In this context, ISIT follows the technology platforms concept, which entails defining standard process flows that can be used to manufacture a large group of components simply by varying certain design parameters. Applying this modular technology concept is the optimal way to ensure that ISIT continues to offer competitive prices to its customers.

ISIT services have attractive implications for small-and medium-sized enterprises, which can take advantage of the institute's facilities and expertise in realizing technological innovations up to products.

Electrical test of Lthium polymer batteries.



Wafer with electrical biochips.



Process monitoring at the ISIT lead-free training line.

ISIT presentation at Productronica 05, München.

Customers

ISIT cooperates with companies of different sectors and sizes. In the following some companies are presented as a reference:

AARDEX, Zug, Switzerland

ABB, Västeräs, Sweden

Adaptive Photonics, Hamburg

Airbus-Systeme, Buxtehude

Alcatel Vacuum Technology, Annecy, France

Alma, Lyon, France

Amic, Uppsala, Sweden

Andus GmbH, Berlin

ARC Seibersdorf Research GmbH, Seibersdorf, Austria

ASE, Seoul, Korea

Atotech Deutschland GmbH, Berlin

Atral, Crolles, France

Audi AG, Ingolstadt

Autoliv GmbH, Elmshorn

Baolab Microsystems, Terrassa, Spain

Basler Vision Technologies, Ahrensburg

BDT GmbH & Co. KG, Rottweil

Bosch, Reutlingen

Bullith Batteries AG, München

Cardi plus, Sevilla, Spain

Carl Zeiss SMT, Oberkochen

Condias GmbH, Itzehoe

Conti Temic Microelectronics GmbH, Nürnberg

DancoTech A/S, Ballerup, Denmark

Danfoss Drives, Graasten, Denmark

Danfoss Silicon Power GmbH, Schleswig

Datacon, Radfeld/Tirol, Austria

Degussa AG, Hanau

Diehl Avionik, Überlingen

Diehl BGT Defense, Nürnberg

Dräger Systemtechnik, Lübeck

EADS, Ulm

eBiochip Systems GmbH, Itzehoe

Elmos Semiconductor AG, Dortmund

EN Electronic Network, Bad Hersfeld

Engineering Center for Power Electronics GmbH, Nürnberg

Environics Oy, Mikkeli, Finland

Epcos, München

Equicon, Jena

ESCD, Brunsbüttel

ESW-EXTEL Systems GmbH, Wedel

EVGroup, Schärding, Austria

FOS Messtechnik GmbH, Schacht-Audorf

Fuba GmbH, Gittelde

GPS, Stuttgart

H. C. Starck, Leverkusen

Heidenhain, Traunreut

Hella KG, Lippstadt

Hök Instrument AB, Västeräs, Sweden

IMS, Jena

IMS, Wien, Austria

IngenieurService Dr. Wanders, Neufahrn

JLS Designs, Somerset, UK

Jungheinrich AG, Norderstedt

KC-Produkte GmbH, Friolzheim

Kember Associates, Bristol, UK

Kerr McGee, Krefeld

Kristensen GmbH, Harrislee-Flensburg

Lam Research, Fremont, USA

LEICA, Jena

Litef, Freiburg

Mair Elektronik GmbH, Neufahrn

MED – EL, Innsbruck, Austria

Miele & Cie., Gütersloh

Motorola GmbH, Flensburg

MRT – Micro-Resist-Technology, Berlin

M+W Zander, Stuttgart

Nokia Research Center, Nokia Group, Helsinki, Finland

Novatrans Group SA, Vaumarcus, Switzerland

NU-Tech GmbH, Neumünster

OK Media Disc Service GmbH & Co.KG, Nortorf

Omicron Laserage GmbH, Rodgau

Osram GmbH, München

Osram Opto Semiconductors GmbH, Regensburg

Oticon, A/S, Hellerup, Denmark

PAV Card GmbH, Lütjensee

Peter Wolters AG, Rendsburg

Philips Semiconductors, Hamburg

PlanOptik AG, Elsoff

Polytec GmbH, Waldbronn

PRETTL Elektronik Lübeck GmbH, Lübeck

Protec Process Systems GmbH, Siegen

Raytheon Anschütz GmbH, Kiel

Rehm Anlagenbau GmbH + Co. KG, Blaubeuren-Seissen

Rena Sondermaschinen GmbH, Gütenbach

Robert Bosch GmbH, Salzgitter

SAES Getters S.p.A., Lainate/Milan, Italy

Scana Holography Company GmbH, Schenefeld

Scanbec Oy, Oulu, Finland

Scanbec GmbH, Halle

Schott, Landshut

SEF GmbH, Scharnebek

Sensiron AG, Stäfa, Switzerland

SensorDynamics (SD), Lebring, Austria

Sentech Instruments GmbH, Berlin

Siemens AG, München

Siemens VDO Automotive AG, Schwalbach

Siemens VDO, Karben

Siemens VDO, Babenhausen

SMA Regelsysteme GmbH, Niestetal

Smart Material GmbH, Dresden

SMI GmbH, Itzehoe

SMI, Milpitas, USA

Sollith Batteries GmbH, Itzehoe

Sonion, Lyngby, Denmark

ST Microelectronics, Crolles, France

Still GmbH, Hamburg

ST Microelectronics, Mailand, Italy

SÜSS Microtec AG, Garching

Suunto, Vantaa, Finland

Technion, Haifa, Israel

Technolas, München

Technovision GmbH, Feldkirchen

Telefonica, Madrid, Spain

Thales Avionics, Valence, France

Thales, Paris, France

Treichel Elektronik GmbH, Springe

Trinamic, Hamburg

Tronic´s, Grenoble, France

Vectron International GmbH & Co. KG, Neckarbischofsheim

Vishay Beyschlag, Heide

Vishay, Dimona, Israel

Vishay, Holon, Israel

Vishay Siliconix Itzehoe GmbH, Itzehoe

Vishay Siliconix, Santa Clara, USA

Wabco Fahrzeugbremsen, Hannover

Wirion-Serion-Institut, Würzburg

Woowon Technology, Korea

Innovation Catalogue

ISIT offers its customers various products and services already developed for market introduction. The following table presents a summary of the essential products and services. Beyond that the utilisation of patents and licences is included in the service.

Product / Service	Market	Contact Person
Testing of semiconductor manufacturing equipment	Semiconductor equipment manufacturers	Dr. Gerfried Zwicker + 49 (0) 4821 / 17 - 4309 gerfried.zwicker@isit.fraunhofer.de
Chemical-mechanical polishing (CMP), planarization	Semiconductor device manufacturers	Dr. Gerfried Zwicker + 49 (0) 4821 / 17 - 4309 gerfried.zwicker@isit.fraunhofer.de
Wafer polishing, single and double side	Si substrates for device manufacturers	Dr. Gerfried Zwicker + 49 (0) 4821 / 17 - 4309 gerfried.zwicker@isit.fraunhofer.de
IC processes CMOS, PowerMOS, IGBTs	Semiconductor industry IC-users	Detlef Friedrich + 49 (0) 4821 / 17 - 4301 detlef.friedrich@isit.fraunhofer.de
Single processes and process module development	Semiconductor industry semiconductor equipment manufacturers	Detlef Friedrich + 49 (0) 4821 / 17 - 4301 detlef.friedrich@isit.fraunhofer.de
Customer specific processing	Semiconductor industry semiconductor equipment manufacturers	Detlef Friedrich + 49 (0) 4821 / 17 - 4301 detlef.friedrich@isit.fraunhofer.de
Microsystem Products	Electronic industry	Dr. Ralf Dudde + 49 (0) 4821 / 17 - 4212 ralf.dudde@isit.fraunhofer.de
Plasma diagnostics	Semiconductor equipment manufacturers	Dr. Joachim Janes + 49 (0) 4821 / 17 - 4601 joachim.janes@isit.fraunhofer.de
Etching and deposition process control	Semiconductor industry	Dr. Joachim Janes + 49 (0) 4821 / 17 - 4601 joachim.janes@isit.fraunhofer.de
Ion projection lithography open stencil mask technology and resist processes	Semiconductor industry	Dr. Wilhelm Brünger + 49 (0) 4821 / 17 - 4228 wilhelm.bruenger@isit.fraunhofer.de
Inertial sensors	Motorvehicle technology, navigation systems, measurements	Dr. Bernd Wagner + 49 (0) 4821 / 17 - 4223 bernd.wagner@isit.fraunhofer.de
Design for commercial MST processes	Micro sensors and actuators	Dr. Bernd Wagner + 49 (0) 4821 / 17 - 4223 bernd.wagner@isit.fraunhofer.de
Thick epi poly MEMS processing	Sensors and actuators	Dr. Peter Merz + 49 (0) 4821 / 17 - 4513 peter.merz@isit.fraunhofer.de
Microvalves for gases and liquids	Analytic, medical technology measurement	Hans Joachim Quenzer + 49 (0) 4821 / 17 - 4643 hans-joachim.quenzer@isit.fraunhofer.de
Microoptical scanners and projectors	Biomedical technology, optical measurement industry, telecommunication	Ulrich Hofmann + 49 (0) 4821 / 17 - 4553 ulrich.hofmann@isit.fraunhofer.de
Flow sensors	Automotive, fuel cells	Dr. Peter Lange + 49 (0) 4821 / 17 - 4220 peter.lange@isit.fraunhofer.de
Microoptical components	Optical measurement,	Dr. Klaus Reimer + 49 (0) 4821 / 17 - 4506 klaus.reimer@isit.fraunhofer.de

Product / Service	Market	Contact Person
Mastering and replication of micro structures in plastic	Microoptics, microfluidics	Dr. Klaus Reimer + 49 (0) 4821 / 17 - 4506 klaus.reimer@isit.fraunhofer.de
Design and test of analogue and mixed-signal ASICs	Measurement, automatic control industry	Jörg Eichholz + 49 (0) 4821 / 17 - 4213 joerg.eichholz@isit.fraunhofer.de
Design Kits	MST foundries	Jörg Eichholz + 49 (0) 4821 / 17 - 4213 joerg.eichholz@isit.fraunhofer.de
RF-MEMS	Telecommunication	Dr. Thomas Lisec + 49 (0) 4821 / 17 - 4512 thomas.lisec@isit.fraunhofer.de
MST Design and behavioural modelling	Measurement, automatic control industry	Jörg Eichholz + 49 (0) 4821 / 17 - 4213 joerg.eichholz@isit.fraunhofer.de
Electrodeposition of microstructures	Surface micromachining	Martin Witt + 49 (0) 4821 / 17 - 4613 martin.witt@isit.fraunhofer.de
Digital micromirror devices	Communication technology	Dr. Klaus Reimer + 49 (0) 4821 / 17 - 4506 klaus.reimer@isit.fraunhofer.de
Electrical biochip technology (proteins, nucleic acids, haptens)	Biotechnology, related electronics microfluidics, environmental analysis, Si-Chipprocessing, packaging, chip loading	Dr. Rainer Hintsche + 49 (0) 4821 / 17 - 4221 rainer.hintsche@isit.fraunhofer.de
Secondary lithium batteries based on solid state ionic conductors	Mobile electronic equipment, medical applications, automotive, smart cards, labels, tags	Dr. Peter Gulde + 49 (0) 4821 / 17 - 4307 peter.gulde@isit.fraunhofer.de
Battery test service, electrical parameters, climate impact, reliability, quality	Mobile electronic equipment medical applications, automotive, smart cards; labels, tags	Dr. Peter Gulde + 49 (0) 4821 / 17 - 4307 peter.gulde@isit.fraunhofer.de
Quality and reliability of electronic assemblies (http://www.isit.fraunhofer.de)	Microelectronic and power electronic industry	Karin Pape + 49 (0) 4821 / 17 - 4229 karin.pape@isit.fraunhofer.de
Material and damage analysis	Microelectronic and power electronic industry	Dr. Thomas Ahrens + 49 (0) 4821 / 17 - 4605 thomas.ahrens@isit.fraunhofer.de
Thermal measurement and simulation	Microelectronic and power electronic industry	Dr. M. H. Poech + 49 (0) 4821 / 17 - 4607 max.poech@isit.fraunhofer.de
Leadfree / RoHS transformation in electronic assembly	Electronic industry	Dr. Thomas Ahrens + 49 (0) 4821 / 17 - 4605 thomas.ahrens@isit.fraunhofer.de
Packaging for microsystems, sensors, multichip modules (http://www.isit.fraunhofer.de)	Microelectronic, sensoric and medical industry	Karin Pape + 49 (0) 4821 / 17 - 4229 karin.pape@isit.fraunhofer.de
Wafer level packaging, ultra thin Si packaging and direct chip attach using flip chip techniques	Microelectronic, sensoric and medical industry	Wolfgang Reinert + 49 (0) 4821 / 17 - 4617 wolfgang.reinert@isit.fraunhofer.de
Vacuum wafer bonding technology	Microelectronic, sensoric and medical industry	Wolfgang Reinert + 49 (0) 4821 / 17 - 4617 wolfgang.reinert@isit.fraunhofer.de

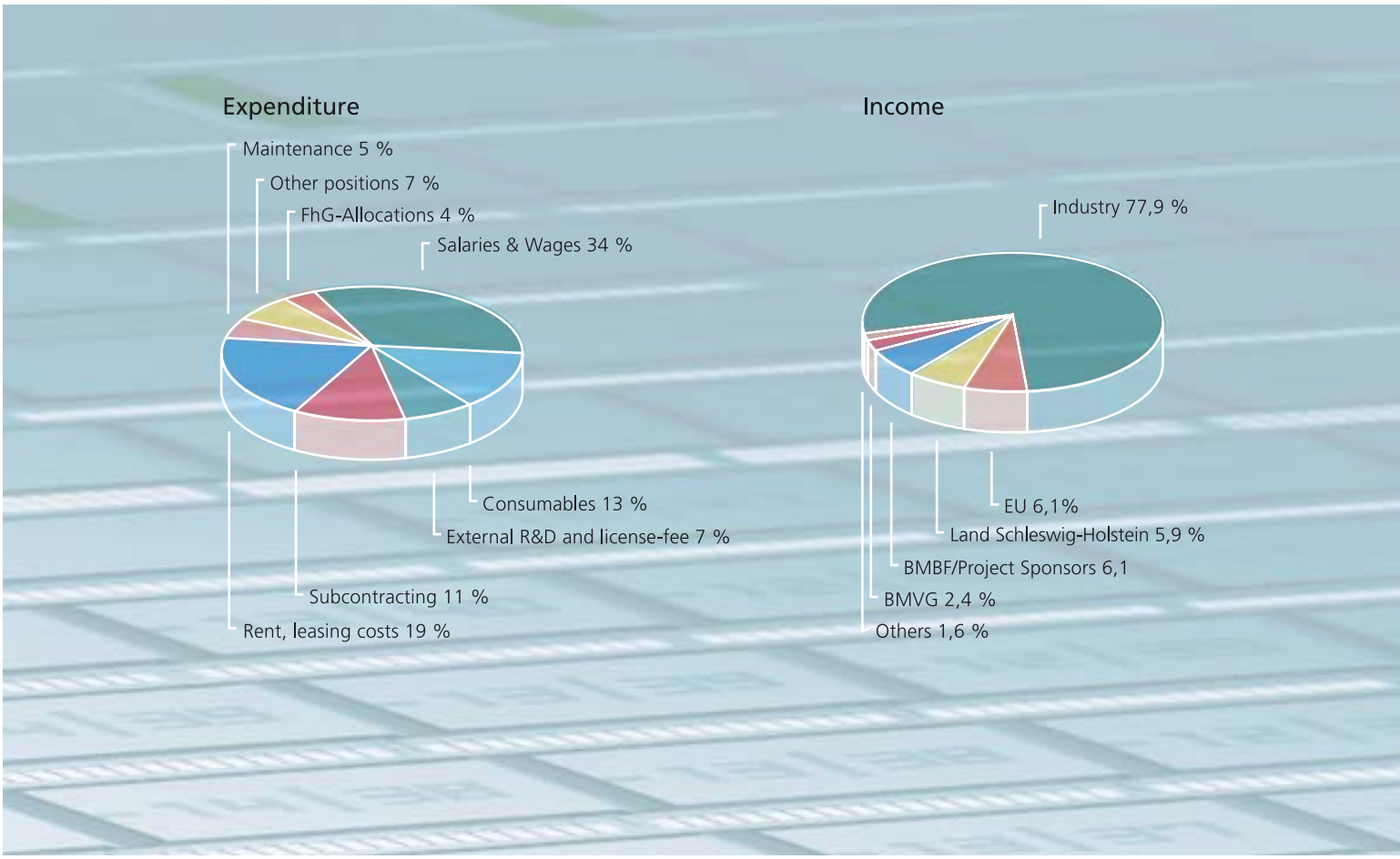
Representative Figures

Expenditure

In 2005 the operating expenditure of Fraunhofer ISIT amounted to 19.968,3 T€. Salaries and wages were 6.840,2 T€, material costs and different other running costs were 13.128,1 T€.

Income

The budget was financed by proceeds of projects of industry/industrial federations/small and medium sized companies amounting to 14.058,5 T€, of government/project sponsors/federal states amounting to 2.595,0 T€ and of European Union/others amounting to 1.388,1 T€.

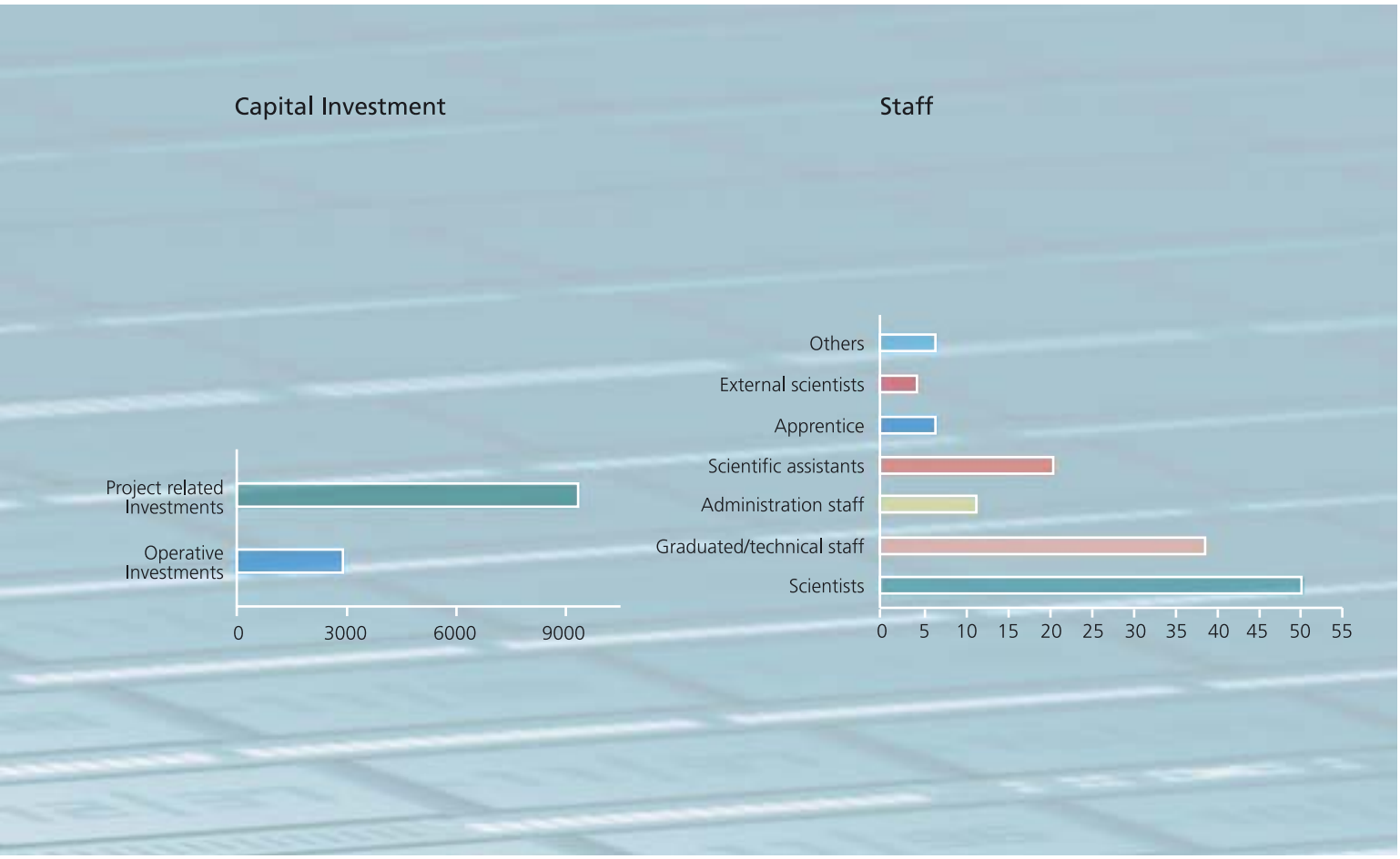


Capital Investment

In 2005 the institutional budget of capital investment was 12.191,6 T€. The amount of operating investment was 2.853,6 T€ and project related investments were amounted to 9.338,0 T€.

Staff Development

In 2005, on annual average the staff consisted of 99 employees. 50 were employed as scientific personnel, 38 as graduated/technical personnel and 11 worked within organisation and administration. The employees were assisted through 20 scientific assistants and 6 apprentices. 4 scientists and 6 others supported the staff as external experts.



The Fraunhofer-Gesellschaft at a Glance

The Fraunhofer-Gesellschaft

The Fraunhofer-Gesellschaft undertakes applied research of direct utility to private and public enterprise and of wide benefit to society. Its services are solicited by customers and contractual partners in industry, the service sector and public administra-tion. The organization also accepts commissions and funding from German federal and Länder ministries and government departments to participate in future-oriented research projects with the aim of finding innovative solutions to issues concerning the industrial economy and society in general.

By developing technological innovations and novel systems solutions for their customers, the Fraunhofer Institutes help to reinforce the competitive strength of the economy in their local region, and throughout Germany and Europe. Through their work, they aim to promote the successful economic development of our industrial society, with particular regard for social welfare and environmental compatibility.

As an employer, the Fraunhofer-Gesellschaft offers its staff the opportunity to develop the professional and personal skills that will allow them to take up positions of responsibility within their institute, in other scientific domains, in industry and in society.

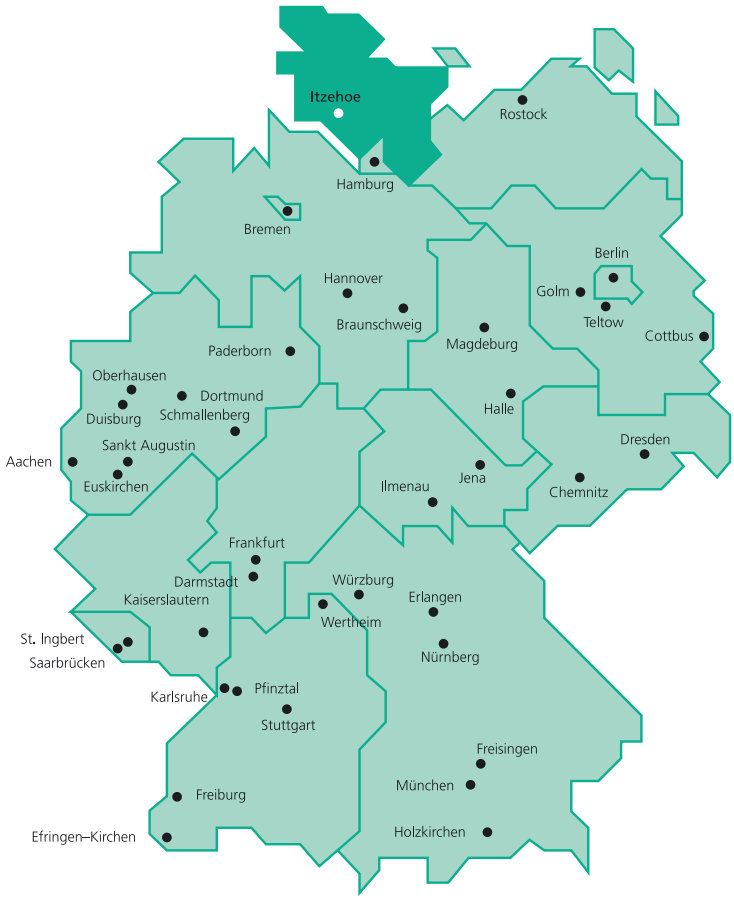
At present, the Fraunhofer-Gesellschaft maintains some 80 research units, includ-ing 58 Fraunhofer Institutes, at over 40 different locations in Germany. The majority of the roughly 12,500 staff are quali-fied scientists and engineers, who work with an annual research budget of over 1 billion euros. Of this sum, more than € 900 million is generated through contract research. Roughly two thirds of the Fraunhofer-Gesellschaft's contract research revenue is derived from contracts with industry and from publicly financed research projects. The remaining one third is contributed by the German federal and Länder governments, partly as a means of enabling the institutes to pursue more fundamental research in areas that are likely to become relevant to industry and society in five or ten years' time.

Affiliated research centers and representative offices in Europe, the USA and Asia provide contact with the regions of greatest importance to present and future scientific progress and economic development.

The Fraunhofer-Gesellschaft was founded in 1949 and is a recognized non-profit organization. Its members include well-known companies and private patrons who help to shape the Fraunhofer-Gesellschaft's research policy and strategic development.

The organization takes its name from Joseph von Fraunhofer (1787–1826), the illustrious Munich researcher, inventor and entrepreneur.

Locations of the Research Establishment



Representative Results of Work

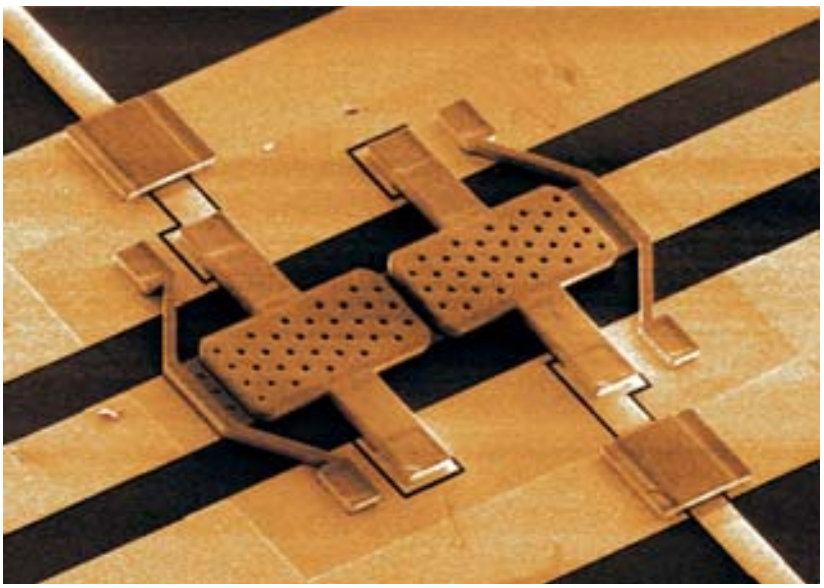
Surface-Micromachined RF-MEMS Devices

Due to the rapidly growing interest in RF MEMS during the last years at ISIT significant effort has been spended on the development of RF switches and varactors. Up to now the major part of the RF MEMS market was for bulk acoustic wave (BAW) devices. But micro-machined resonators and switches would also result in both volume and high-end applications as soon as reliability and packaging problems can be solved.

In the metal surface-micromachining process developed at ISIT for RF switches and varactors both issues are considered. Nickel is used as the main material to build up the free standing structure. The high Young´s module of Ni provides good mechanical properties. Due to the high thermal stability of Ni the free standing structure withstand heat treatments at up to 450° C without electrical or mechanical degradation. This is of great importance in terms of wafer-level packaging procedures usually requiring 300° C and above.

By introducing compressive stress in the membrane of the device with additional upper electrodes shown in figure 1 varactors with a tuning range of several pF can be obtained. Due to the stress the membrane takes up a kind of s-shape touching upper electrodes and the signal line at the same time.

Sputtered AlN has been introduced as dielectric in the active area of capacitive RF switches like shown in figure 2. Under certain conditions this material allow a switch



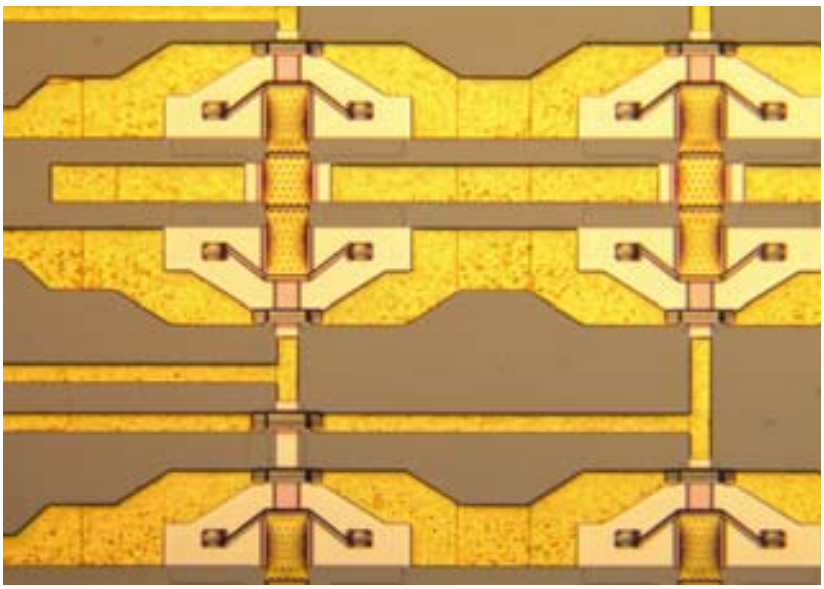


Figure 1: Photo and REM picture of a device acting as variable capacitor. The thin Ni membrane is free movable between the signal line below and the thick Ni electrodes above.

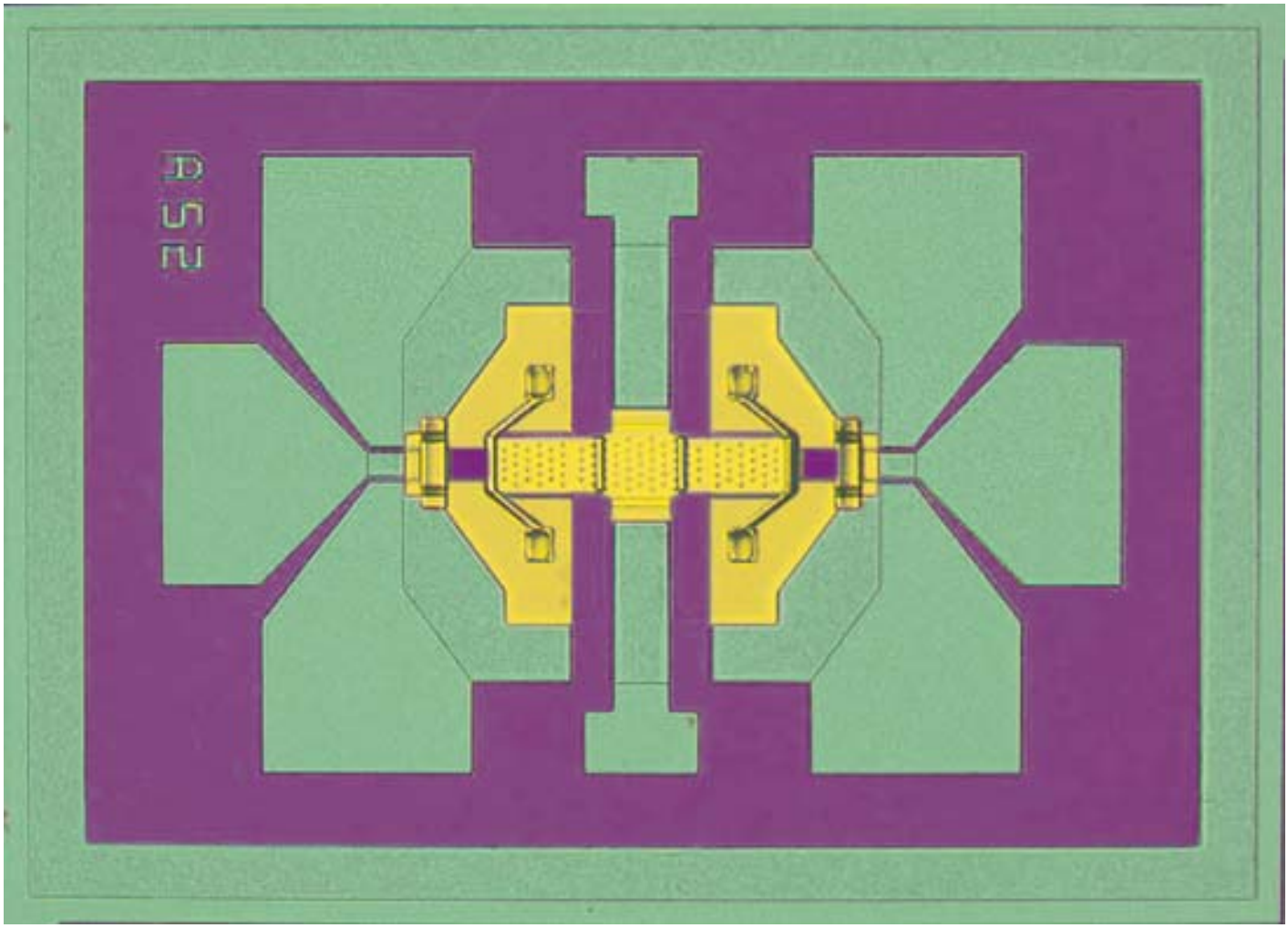


Figure 2: Photo of a capacitive RF-MEMS switch. The thin Ni membrane is supported by thick spring-type Ni anchoring structures compensating thermally induced stresses. To avoid high voltages on the signal line electrically isolated actuation electrodes are embedded in the ground area.

operation without charge induced sticking of the membrane using unipolar DC voltages only. Up to now, total on times of more then 1500 hours without failure have been demonstrated. The on-capacitance of switches with a typical AlN thickness of 300 nm is in the range of 160-180 pF/mm^2. For air gaps of 2-3 µm between membrane and signal line on-off ratios in the range of 15-30 can be expected.

Electrical Feedthroughs Using Wafer-Level Glass-Flow Technology

The use of feedthroughs in wafer-level packaging allows the construction of hermetic encapsulations with very small footprints. In combination with flip-chip assembly, chip stacking concepts can be realized for high-density electronic subsystems.

In the EU-funded VABOND project (IST-2001-34224), a new feedthrough technology has been developed and applied to passive wafer caps (figure 1), like they could be used for inertial sensor MEMS. The process is mainly based on the viscous glass flow process (GFP) that was earlier described for the manufacturing of micro lenses. The novelty here is to fabricate a composite wafer consisting of conductive silicon structures embedded in insulating glass areas.

The glass flow process steps are shown in figure 2: First, a patterning process forms deep silicon structures. Then, an anodic silicon/glass wafer-bonding is effected under vacuum. Becoming viscous during high temperature annealing, the glass flows into the cavities of the silicon wafer. The necessary matching of thermal expansion coefficients in the wafer stack is

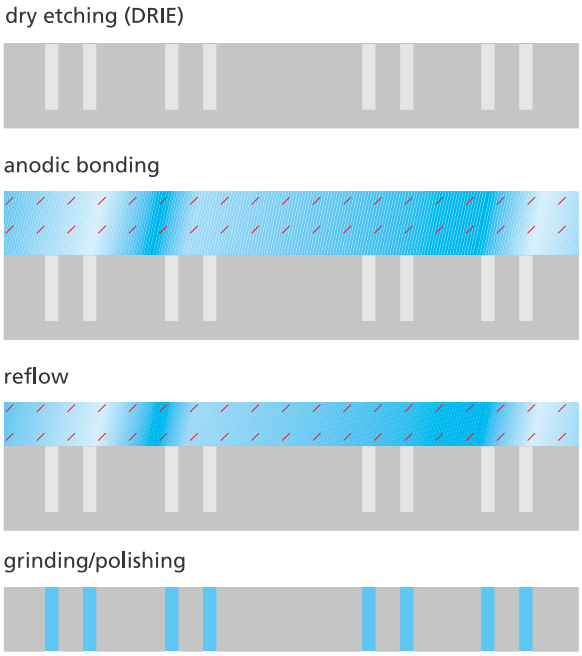
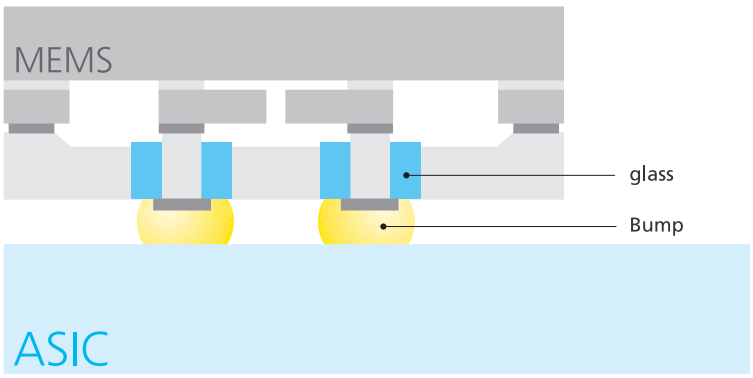


Figure 2: Process scheme for the fabrication of composite silicon / glass wafers: After deep structuring, the silicon wafer is sealed under vacuum with a cap wafer. The viscous glass flow fills the cavities during an annealing step. The remaining silicon base and the glass layer are removed by grinding and polishing.

Figure 1: Electrical feedthroughs in the cap wafer enable the use of flip chip process for the connection of MEMS to the external electronic circuits.



achieved with Borofloat 33© glass wafers. Finally, the cap wafer is completed by grinding and polishing both sides of the wafer stack.

Two approaches have been realised to produce vertical silicon conductors, a mechanical process and deep reactive ion etching (DRIE). The mechanical process uses a dicing saw and issues a regular array of silicon pillars with typical dimensions of 120 µm x 120 µm and a height of 600 µm. A remaining closed ring near the wafer edge (8 mm distance) allows the hermetical sealing of the wafer stack, which is a must for the glass flow process. In this approach, over 90% of the silicon wafer is replaced by glass (figure 3a to 3c). – In the second approach, the silicon wafer is structured using deep reactive ion etching (DRIE). Here, feedthroughs consist of only small insulating glass rings around a central silicon pin ("donut" structure).

Since N-doped silicon wafers with a resistivity of 20 m Ω*cm were used as a substrate material, a resistance of approx. 12 Ω was measured for pin-type feedthroughs with dimensions of 100 µm x 100 µm (500 µm thickness). Using silicon

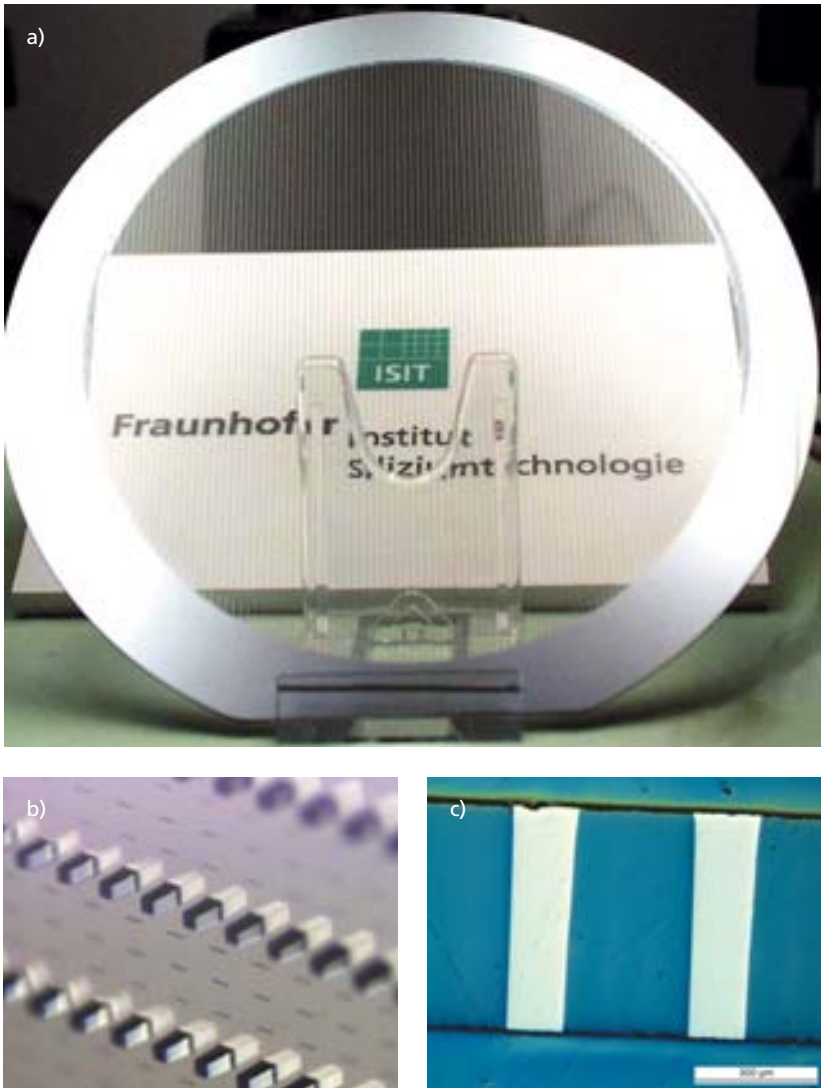


Figure 3:
a) Picture of a complete composite 6" silicon / glass wafer: Small silicon islands fabricated by dicing are embedded in a glass matrix. Due to the glass flow process the composite silicon/ glass wafer is surrounded by a silicon ring.
b) The microscopic view shows square silicon pillars (produced by dicing saw) in a glass matrix.
c) Cross section of the wafer from figure 2 – The glass flow process results in very tight bonds between the glass (dark areas) and the silicon (light areas, about 550 µm thick).

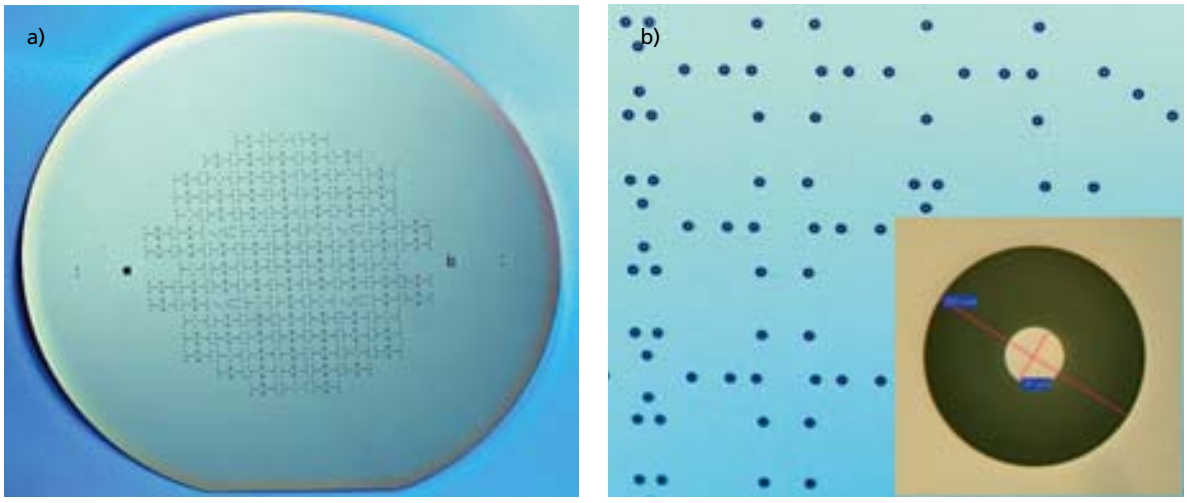
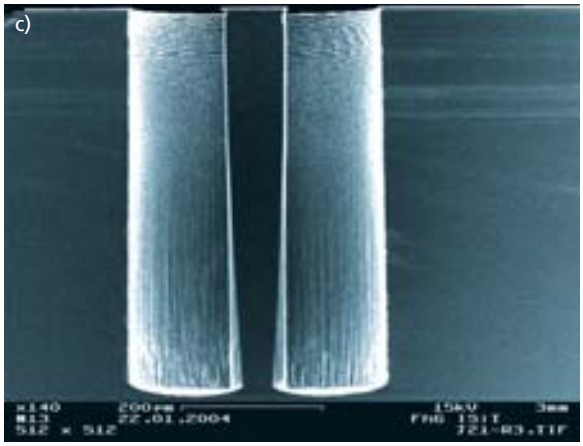


Figure 4: a) and b) Ring type silicon/ glass wafer – Small "donut"-shaped glass rings surround a silicon centre pin which forms the feedthrough contact.



c) The donut structures are etched approx. 550 µm deep into the silicon wafer. Filling the donut structures was more difficult than using pin type wafers.

wafers with a resistivity of 2 mΩ*cm should allow to achieve a resistance of 1-2 Ω per feedthrough.

For the first bonding tests with glass/silicon pin-type feedthroughs, a eutectic gold/silicon bonding process was applied using a sputtered 1 µm gold film. The lithography and chemical wet etching produces a contact metallization on the silicon pins and a sealing frame in one step (figure 6). The gold layer and the silicon of the pins form an alloy that wets the gold pads (dark structures in figure 5 and figure 6). The gold of the surrounding frame remains unaffected.

Since the feedthrough wafer must guarantee a hermetic sealing on a device wafer, leakage tests are essential. In a first approach, a simple test procedure was applied (figure 7), using different samples of pin-type glass / silicon wafers. These were mounted on the inlet vacuum flange of a helium leakage tester (using a conventional 20 mm viton o-ring) and flushed with Helium gas. Helium diffusion either through leaks of the samples or through the o-ring itself was distinguished by reference measurements and a test leak sample. Thus, the minimum resolution of this approach was determined to approx. 10^{-9} l mbar/s for the considered area. Since the detection area in this set-up covers up to 1000 feedthroughs, the detection limit per single feedthrough lies at approx. 10^{-12} l mbar/s.

The experiments showed that samples annealed during the glass flow process for less than 4 h had a detectable leakage, while samples annealed for at least 6 h showed no significant helium leakage within the detectable range.

Beside the use of the composite silicon / glass wafers as feedthrough for MEMS devices, various further applications are possible, like thermal isolations inside MEMS chips or the realisation of optical packages.

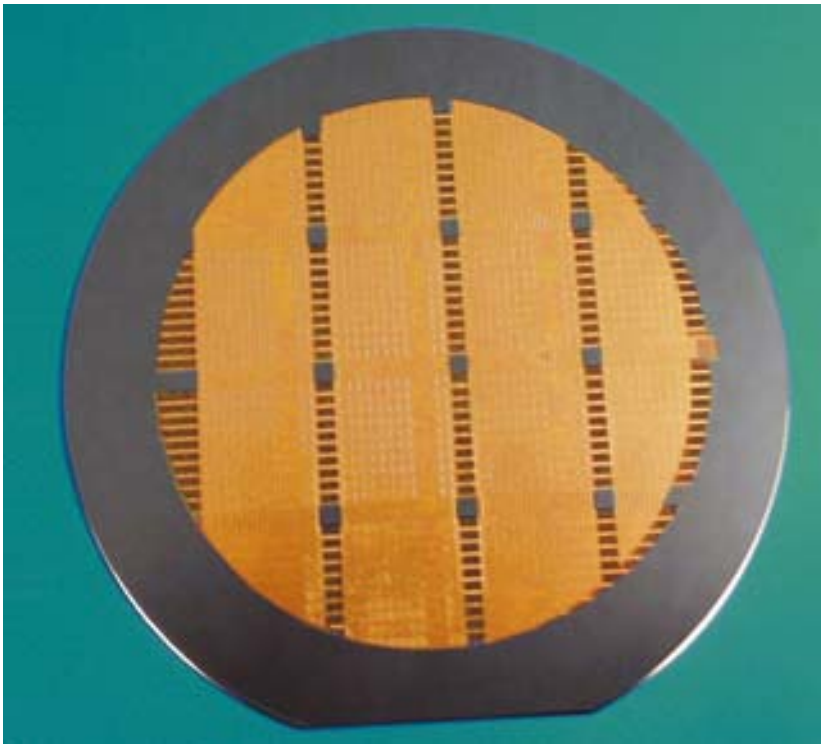


Figure 5: First bonding of a pin-type feedthrough wafer with a silicon wafer. The second wafer was covered with a gold layer (1 µm thick), while on the composite Si/glass wafer the silicon pins were also covered with gold.

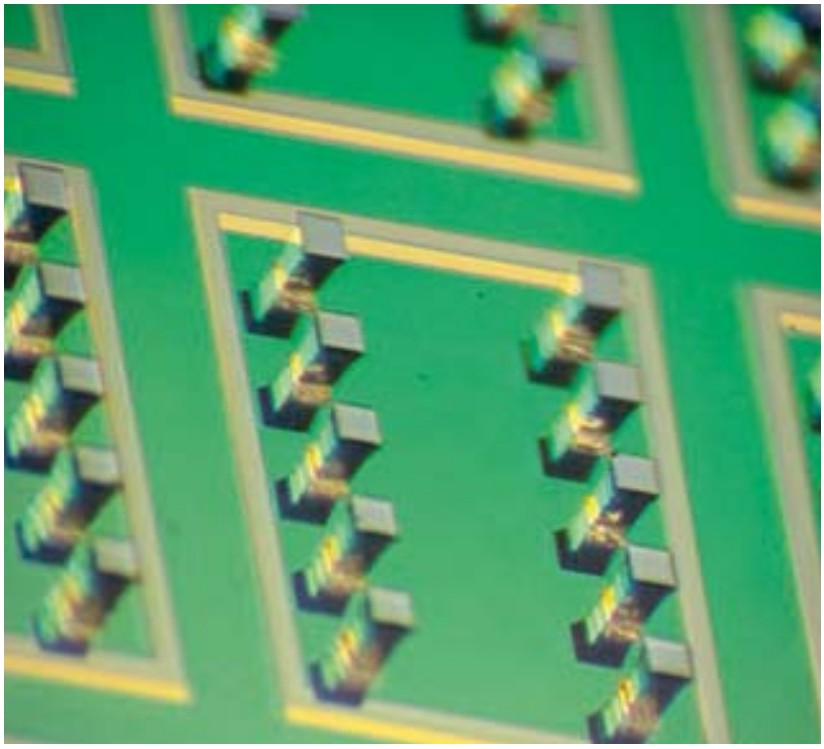


Figure 6: In this experiment, a feedthrough wafer was bonded on a wafer with gold pads. Both the silicon pins and the pads on the second silicon wafer were covered with 1 µm thick gold. Due to the reaction of the silicon in the pins, a gold/silicon alloy is formed during the bonding process and covers the pads.

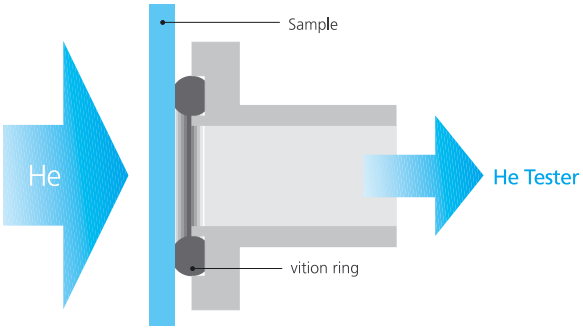


Figure 7: Scheme of the experimental set up to measure the leakage of different feedthrough samples.

Development of High-Speed Wafer-Level-Endtest for Micromechanical Angular-Rate-Sensors

Since more than three years Fraunhofer ISIT is working, in close cooperation with the system-provider SensorDynamics AG, on the development and industrialization of micromechanical angular-rate sensors for automotive applications.

The sensor concept is based on a rotational, resonant in-plane oscillation of the outer ring around a centered anchor point. By applying an angular rate along the sensitive axis the ring and the inner plate is excited to an out-of-plane oscillation due to Coriolis law. The amplitude of this oscillation is proportional to the angular rate. To increase driving momentum at minimum driving voltage the sensor is encapsulated under vacuum on wafer level. More than 1500 sensors are placed on a single 6"-wafer and have to be tested within a short amount of time to reduce costs and to be competitive on the market.

So one of the most challenging tasks is to establish a high speed wafer level endtest which covers all quality related sensor parameters. The characterization takes place on automatic SUESS wafer probers on which each single device is contacted step-by-step by a special probe card.

After getting in electrical contact the test electronic applies a set of test signals which forces the sensor to interact. A readout electronic, integrated on the probecard, converts the sensor response and transmitts the data into a computer to extract the required information.

Special testalgorithms computes mechanical parameters like resonance frequencies, cavity

Figure 1:
Model of an micromechanical angular-rate sensor for automotive applications.

Figure 2:
Sensor devices with and without Si-encapsulation on wafer level.

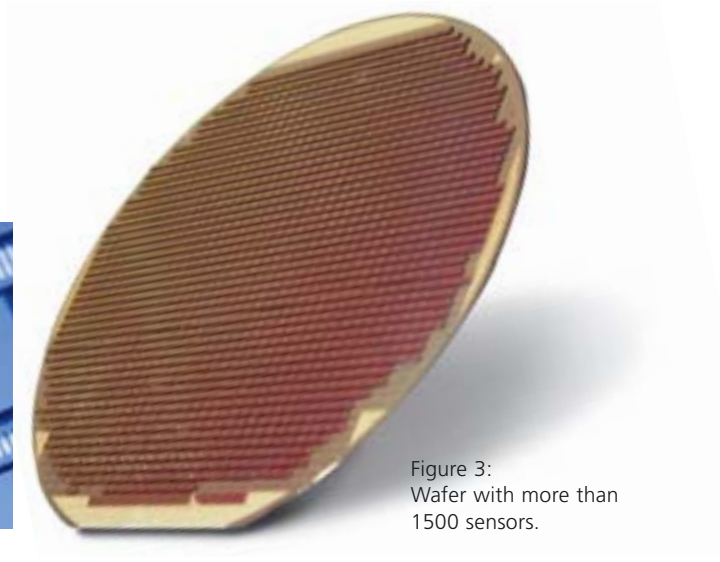


Figure 3:
Wafer with more than 1500 sensors.

Figure 5: Wafer level endtest setup.

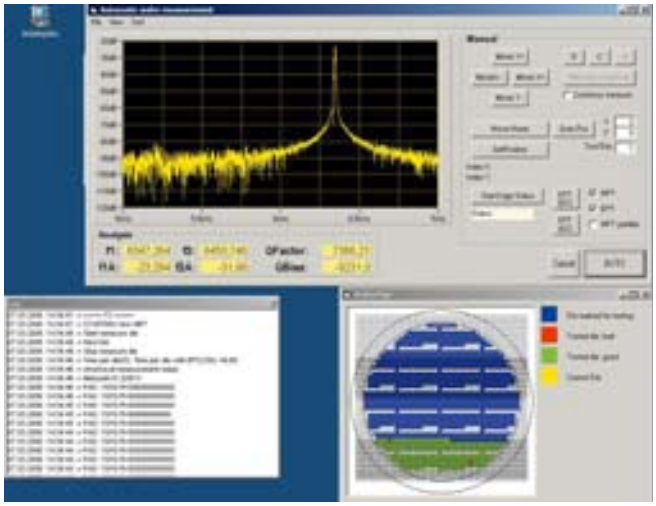


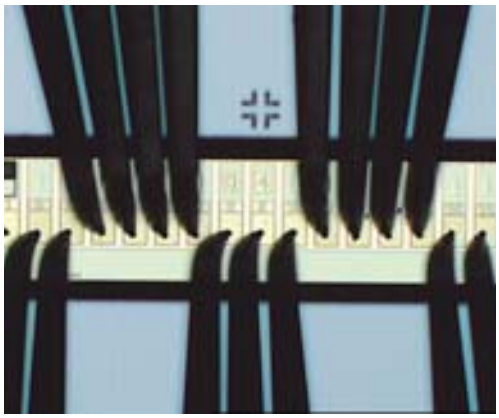
Figure 6: Graphical User Interface of the automatic wafer endtest.

preassure and parasitic coupling effects. An additional test sequence characterizes the electrical behaviour of the sensor.

The overall test time of one wafer is actually in the range of 12 hours at 1500 dies per wafer.

Further inverstigations are to reduce this time down to 2 – 4 hours. This can be achieved by optimizing the test procedures based on intelligent adaptive test strategies and algorithms. In addition a parallelization is planned to test two or more devices per needle card contact.

Figure 4: Needles of the probecard in contact with the sensor pads.



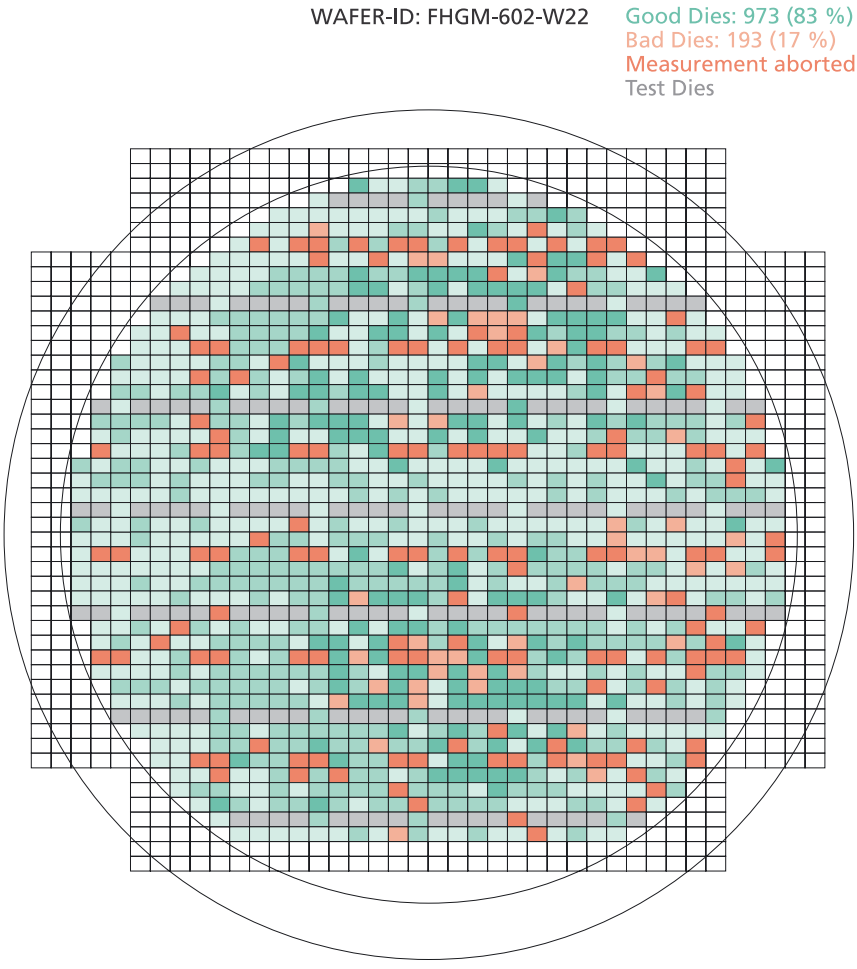


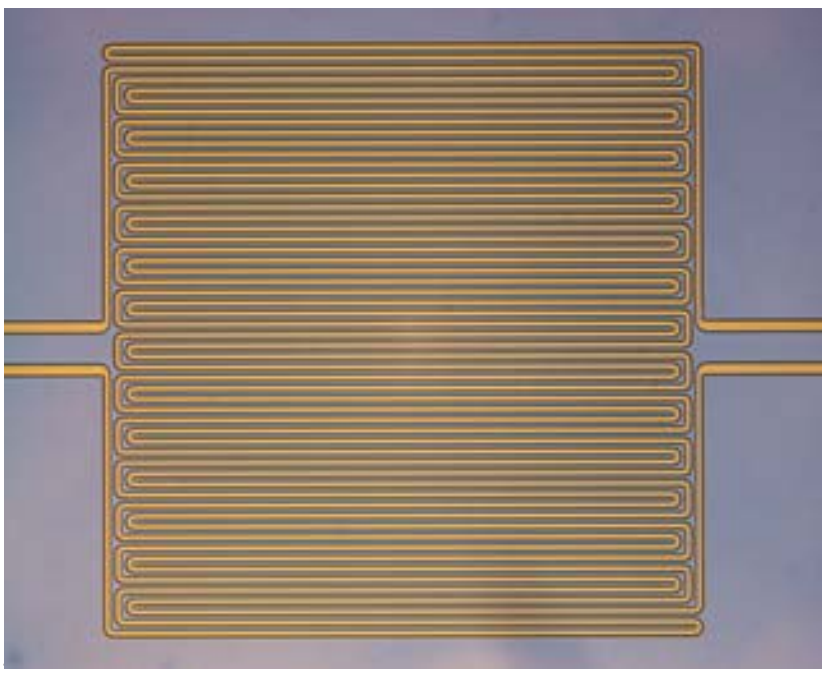
Figure 7:
Wafermap of a tested MEMS wafer.

Ti/TiN and TiN Micro-Heater for High Temperature MEMS

Abstract
We have studied micro heaters made of Ti/TiN stacks and pure TiN layers on bulk micromachined membranes. Ti/TiN stacks show a thermal stability up to 380 °C. The pure TiN heater could reach temperatures up to 600 °C without degradation. Stability is meant in that clause that no phase transitions or interaction with ambience of the material in question occurs in the observed temperature range.

These layers are suitable for sensors in which a high temperature provided by microheaters is necessary, for example gas sensors or IR sources for µ-spectrometer. For the application as anemometric and calorimetric flow sensors it could be shown that a resistance drift does not occur after exposition to elevated temperatures.

Figure 1: Meander structure of two resistance lines with 5 µm lines and spaces on a thin membrane.



Introduction
New conductive layer for heating and sensing in MEMS (Microelectromechanical System) devices operated at elevated temperatures are reported. These micro heaters are formed on membranes for fast response and thermal isolation to the chip frame. In applications such as calorimetric and anemometric flow sensors, gas sensors and IR sources the resistors are heated by a current flow. Thereby they have to withstand temperatures of several hundreds degree of Celsius. Degradation effects in the resistors have to be prevented, otherwise the external/internal signal conditioning circuit could not work properly. The fabrication of such devices in conjunction with standard CMOS processes shows considerable advantages as monolithic integration, low cost production and short cycle times. A variety of metals like Cr, Au or Pt are applied up to now in MEMS devices for this purpose. However, they are exhibiting the disadvantage of being mostly not compatible to IC processing. In this respect polysilicon is the most applied material, but shows some altering behaviour at elevated temperatures. The refractory metals, for example Ta, W, Ti, are also providing candidates for this purpose. But many of these materials are highly reactive at elevated temperatures or show other drawbacks, for example a complicated process management, so the possibilities of choice are rather limited. Ti and TiN thin films are state of the art technology in MOS devices as diffusion barrier between Si and Al or Cu. Because of this proven compatibility with front end MOS technology we have investigated Ti/TiN layers and pure TiN layers for the application as heating and sensing elements. For the protection against inter-diffusion/oxidation effects the Ti thin films were covered with thin TiN layers.

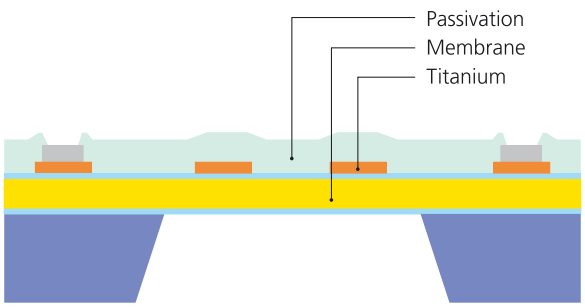


Figure 2: Cross-section of the membrane.

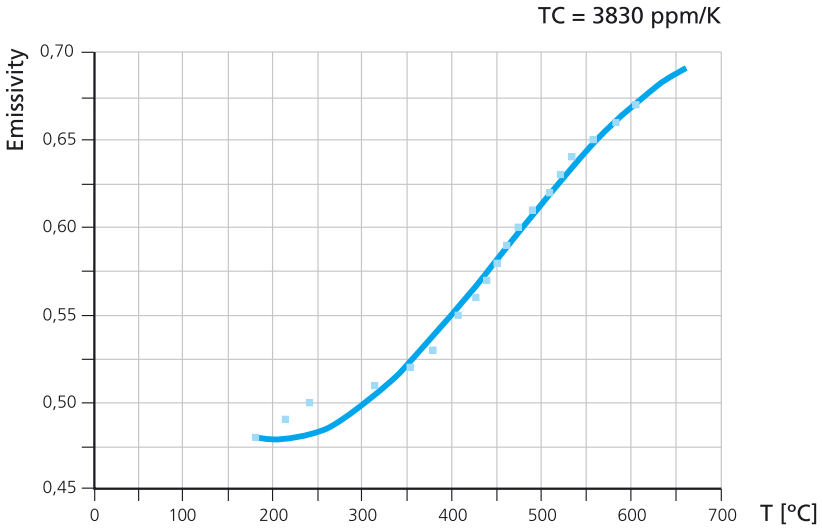


Figure 3: Emissivity as a function of temperature of a chip mounted on a heating block. The chip was completely processed except membrane etching to assure a good heatconductance.

Experimental

All experiments were carried out in a conventional MOS line on Si-wafers with <100> orientation and 150 mm in size. The Ti /TiN thin film consists of a sandwich of 25 nm TiN, 650 nm Ti and 50 nm TiN. These layers and the pure TiN layers of 500 nm thickness were deposited in a reactive sputtering process (poisoning mode) on a stack of $Si_3N_4/SiO_2/Si_3N_4$ with a total thickness of 1 µm. The contact pads were covered with Aluminum for bonding reasons. After structuring the film via lithography and anisotropic dry etch processes the resistor lines are meanderlike with lines and spaces of 5 µm (figure 1). Subsequent a passivation layer of 1 µm thickness was deposited by a plasma enhanced chemical vapour deposition process (PECVD). The membranes were formed by KOH anisotropic wet etching from the backside of the wafer. The size of the membrane is 1.2 mm by 1.3 mm. A drawing of the cross-section is given in figure 2. With this design a good thermal isolation to the chip-frame and a fast thermal response is assured. The temperature coefficient (TC), the resistivity and the response to elevated temperatures were examined. The TC of these materials was measured on a wafer prober with a heatable „hot-chuck“ and compared later on with a measurement in a climate chamber. Within the measurement accuracy no significant deviations were observed. Additional measurements for the high temperature range have been performed using an IR imaging system. The resistivities were calculated from the measured sheet resistances using a conventional 4-point prober.

Temperature stress

The desired temperatures were adjusted by a current flow through the heating resistances. Thereby a voltage was imposed and continuously increased up to a maximum and decreased back to the starting value. This was measured with a parameter analyser and is shown examplarily in figure 5, where the endpoint of the imposed voltage is stepwise increased from 21 to 30 V. The temperature was estimated in a first approximation by extrapolating the linear dependence of the TC.

This calculation from electrical data is only allowed if two aspects are considered: a material degradation (or any change in the materials structure) as effected by the imposed temperature.

This can be excluded, if the resistance remains constant

- after several high temperature cycles up to the same maximum value
- after continuous current stress at the reversible maximum voltage

The second aspect is related to a linear behaviour of the TC over a wide range of temperatures. The resistance-temperature dependence could only be measured until 240 °C, because of experimental limitations of the hot chuck prober. A linear extrapolation beyond this range can be questionary.

Therefore additional measurements have been done by thermography using an infrared imaging system. This system is equipped with a scanner head and an optical telescope, which makes it possible to observe small areas with high resolution. The direct measurement of the temperature by thermography is difficult because of the unknown emissivity of the chip, respectively the chip surface.

The following experimental set up has been used to measure the emissivity. Thereby the chip was mounted on a large iron block, which could be heated up to 700° C. A fully processed chip without membrane etching has been chosen. The reason was an assurement of a good thermal conductivity between the heater block and the chip. The temperature of the iron block has been measured with a thermocouple and the thermal image of the membran area with the resistance lines has been adjusted to this value under variation of the emissivity. We received values for the emissivity between 0.5 and 0.65 for a temperature range of 300° C to 600° C as is shown in figure 3.

Results and Discussion The Ti/TiN stack

The temperature dependence of the resistance R is shown in figure 4. The temperature covers a range from 30° C to 240° C and shows an extremly linear dependence with a correlation factor higher than 0.99. The TC (α) was calculated from such a measurement according to the following equation.

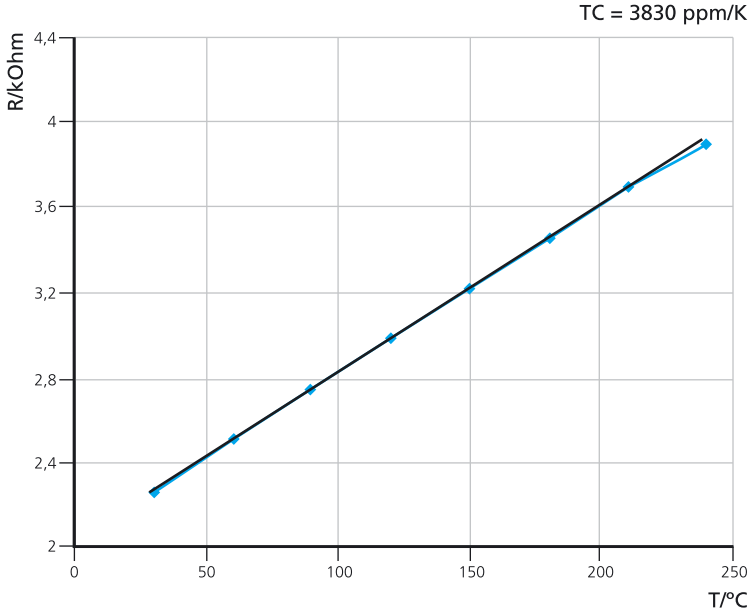


Figure 4: TC measurement of a Ti/TiN resistance.

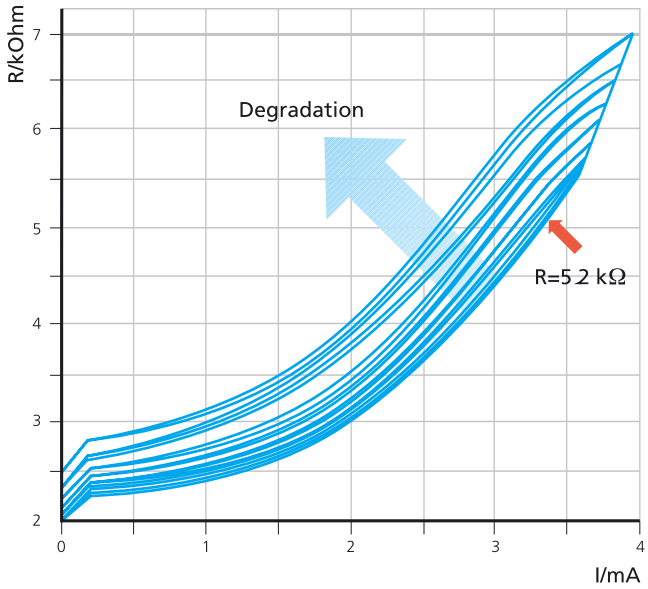


Figure 5: Resistance characteristic (R/Ω vs I/A) for the Ti/TiN lines. The endpoint of the imposed voltage is stepwise increased from 21 to 30 V. The scaling on the I-axis is from 3.9 µA to 4.0 mA. Reversibility is given until R = 5.2 kΩ according to T = 380° C.

$R(T) = R(T_0) * (1 + \alpha(T - T_0))$

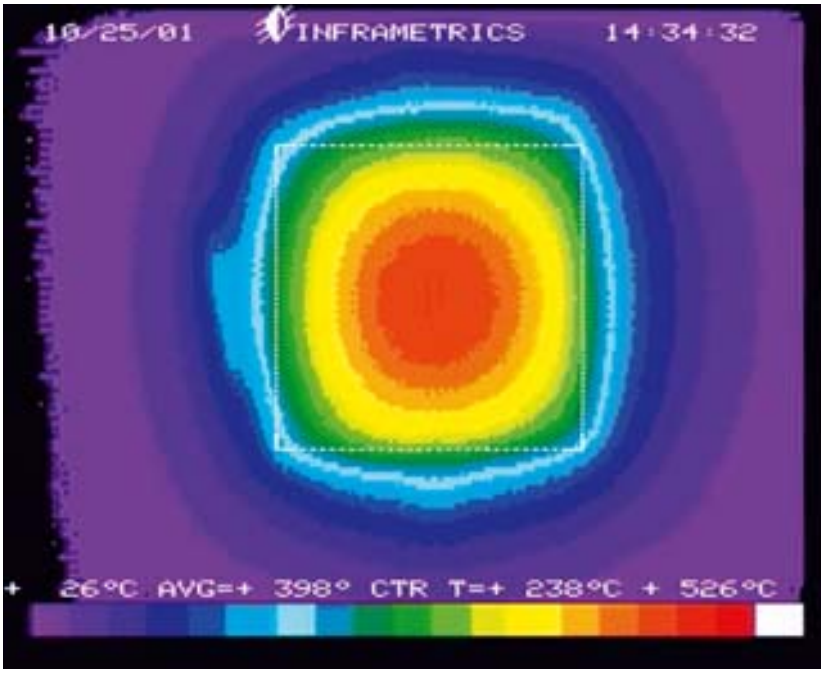
R = resistance (or any physical property),
T = temperature,
T0 = reference temperature
α = temperature coefficient (TC) in the temperature range
$\Delta T = T - T_0$; α is given in 1/K or K^{-1}.

For the Ti/TiN stack a value of 3830 ppm/K (22 – 240° C) was measured. This agrees well with reported data of 3800 ppm/K given for the range of 0 – 100° C. The resistivity was measured with 44 µΩcm and fits also to reported data in the range of 40 to 54 µΩcm. So far these properties of thin film Ti reveal no significant difference from those of bulk Ti.

Performing the temperature stress experiments we achieved a highest temperature of 380° C under reversible conditions. This value corresponds to 5.2 kOhm and was calculated using the TC value from the above mentioned measurement extrapolating linearely from the lower (22 – 240° C) to the upper temperature range (T > 300° C). Also a 24 h current-stress at this temperature has not changed the value of the resistance. Above 380° C a distinct degradation of the resistance could be observed (figure 5). The initial resistance has changed after the sweep cycle. This change is increasing with increasing voltage. Then also a change in the TC occured. This is a clear indication for a material transformation in the Ti/TiN layer.

The temperature of the resistance lines was confirmed independently by the thermographic method. Thereby the resistance lines were internally heated through a current flow to a value of 5.2 kΩ according to the calculated temperature of 380° C. The emissivities ε(T) of the chip were measured by the method described above. As an example, by using these emissivities we measured the temperature of the

Figure 6: Infrared image of the membrane (area between the dashed lines), internally heated. The mean temperature of 398° C is an integrated value over all areas with different temperatures.



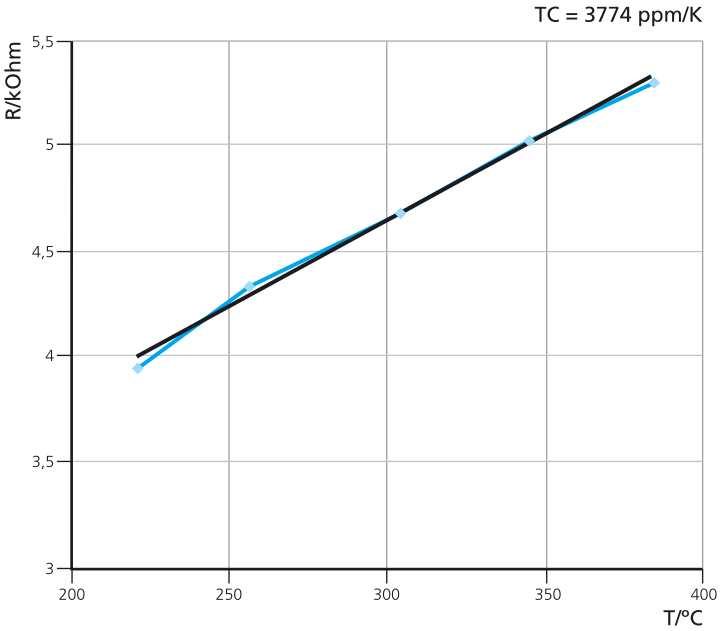


Figure 7: Measurement of the temperature coefficient TC by external heating of the chip.

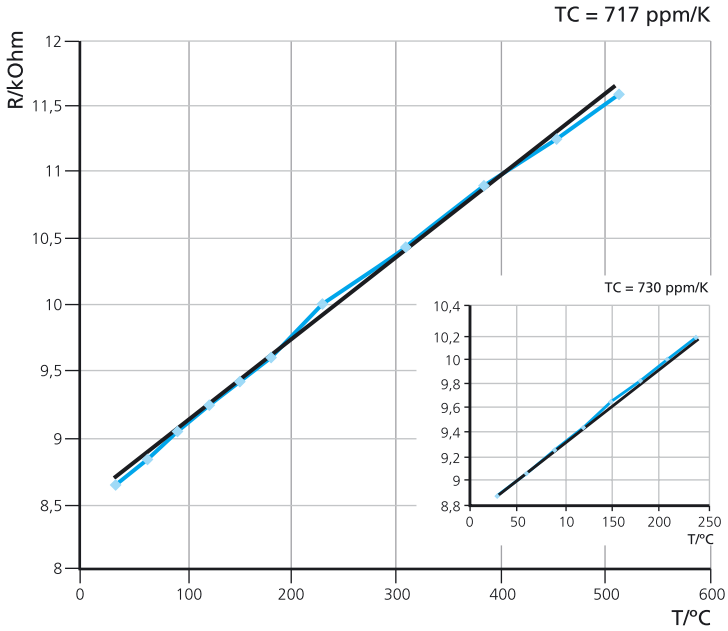


Figure 8: Calculation of the TC of TiN from the temperature dependence of the resistance for internal heating (30° C–180° C) and external heating (230° C–520° C). In the inlet the calculation of the TC from internal heating (30° C–240° C) only is shown.

resistance lines with 398° C. However, internal heating produces a strong temperature gradient from the center of the heater area to the edge. Therefore the mean temperature of 398° C (AVG in figure 6) is an integrated value over the whole membran. The temperature in the center temperature exceeds 526° C and goes down to 238° C beyond the edges of the membrane. This is a consequence of the geometrical size of the heating lines (figure 1). Within this limitation a good agreement between both methods of temperature measurement was obtained. In consequence this also true for the measured resistance, which appears as a mean value. We have calculated the TC again, the result is given in figure 7 with an TC value of 3774 ppm/K. Considering that the temperatures are means, the agreement with the low temperature TC is convincing. This result clearly shows the appropriateness of a linear extrapolation beyond the initially measured temperatur range for this material.

The TiN layer

The temperature dependence of the resistance R for the TiN layer with 500 nm thickness measured on the „hot chuck“ is shown in the inlet of figure 8. Again, the temperature covers a range from 30° C to 240° C and shows also an extremly linear dependence with a correlation factor higher than 0.99. The TC of this layer was calculated with 730 ppm/K and is reported the first time. The resistivity was measured with 115 µΩcm in agreement with published data. Temperature stress was possible until 600° C, at higher temperatures a degradation in the passivation layer occured. This is attributed to a different distribution of the mechanical stress in this stack compared to the above mentioned Ti/TiN stack, which contains a large amount of Titanium. This is supposed to attribute to a stress relaxation in the stack. A hysteresis was never observed (figure 9). The calculated temperature from interpolating the linear dependence of the TC has been verified again by thermography measurements. The chip was heated externally

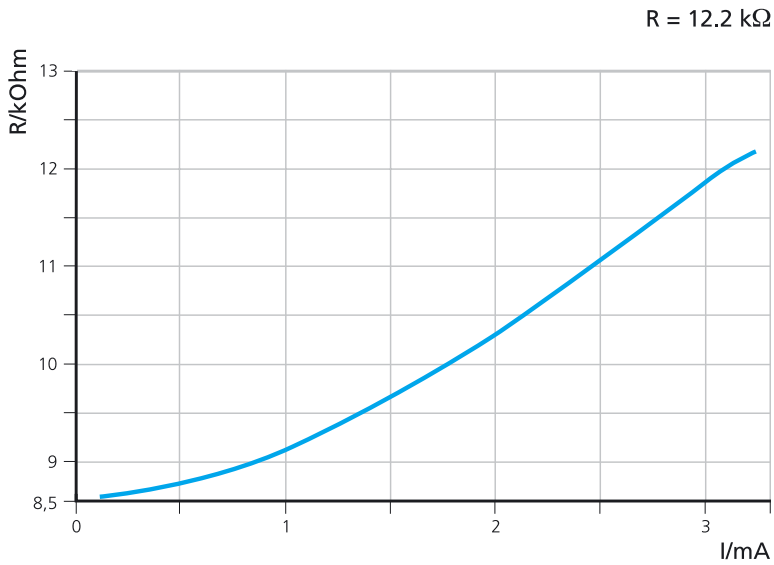


Figure 9: Resistance characteristic (R/Ω vs I/A) for the TiN lines. Reversibility is given until R = 12.2 kΩ according to T = 600° C.

up to that point when the resistors reached 12 kOhm. The IR image together with the corresponding emissivities revealed a value of about 600 °C for this resistance. These values have been estimated under the above mentioned limitations, so the reported data of the resistance and temperature are means. The TC (717 ppm/K) calculated from the whole temperature range (the internal heating from 30 – 180 °C and the external heating from 230 – 520 °C) is shown in figure 8 and reveals no significant deviation from those calculated from the lower temperature range (730 ppm/K). The overall agreement is excellent considering the limitations in the accuracy of the high temperature determination. Thus it can be concluded, that for TiN it is also appropriate to extrapolate the linear behaviour of R(T) beyond the lower temperature range. However, so far the membran was undestroyed, even higher temperatures up to 800 °C have been observed, without a change in the initial resistance at room temperature after switching off the heating current.

Conclusion

Overall Ti and TiN show excellent characteristics. Both are compatible with CMOS technology and can easily be converted from standard processes. A linear dependence of the TC from temperature over a wide range of temperatures has been shown for Ti/TiN and TiN. If a high TC is desired, the Ti/TiN stack can be selected for temperatures of max T = 380 °C. This is usefull for sensor systems related to temperature measurements in moderate hot environments for example calorimetric and anemometric flow sensors and an electrical drift has to be avoided. For heating purpose only, the material of choice is the pure Titaniumnitride layer, since it withstands temperatures of at least 600 °C without material degradation. These heaters could be used for example as reliable IR source for µ-IR spectrometers or they could provide the necessary temperature for the onset of the ionic conduction in solid state gas sensors.

Fieldstop Trench IGBTs with Laser Annealed Backside Emitter

IGBTs (Insulated Gate Bipolar Transistor) are the preferential power switches for the higher voltage range above 400 V. Compared to PowerMOS devices IGBTs benefit from lower conduction losses in the high voltage regime due to the conduction modulation of the low doped drift zone region.

Generally three types of IGBTs are distinguished as shown in figure 1: Punch Through IGBT (PT-IGBT), Non Punch Through IGBT (NPT-IGBT) and Fieldstop IGBT (FS-IGBT). All those IGBTs are different by the Si-substrates used with additional epitaxial- or ion implanted layers.

PT-IGBTs using epitaxial drift zone- and fieldstop-layer grown on highly doped p-substrates. The drawback is the low turn–off speed due to the high Emitter efficiency which has to be overcome by carrier life time adjustment. Since the drift zone is defined by the epitaxial layer there is no need of excessive substrate thinning.

NPT-IGBTs are fabricated on homogeniously doped substrates having the drift zone doping concentration. In order avoid high saturation voltages V_{CEsat} with increased conduction losses the substrate has to be grinded as thin as being required by the maximum break down voltage. Since the Emitter has to be implanted after substrate thinning the switching speed can be adjusted by the Emitter efficiency. No special carrier life time adjustment is required.

The Fieldstop Trench IGBT is currently the most interesting device which can be regarded as a combination out of PT- and NPT-IGBT. Due to a PT-like trapezoidal electrical field distribution the drift zone region can be reduced in thickness by 30 % compared to NPT-IGBTs which is resulting in reduced conduction losses with lower saturation voltage V_{CEsat}. The turn-off speed is dominated by the Emitter efficiency as in the NPT case without any carrier life time reduction.

The challenge of FS-IGBTs especially for 600V and below is the processing of ultrathin wafers since FS-layer and Emitter have to be formed after backside grinding down to 50 – 70 µm.

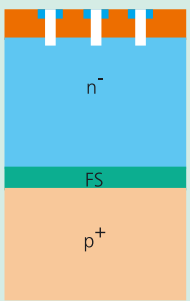
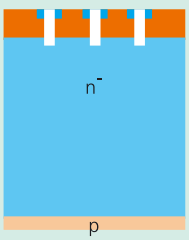
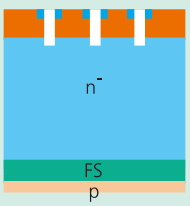
	PT-IGBT	NPT-IGBT	FS-IGBT
Substrate	p^+	n^-	n^-
Drift zone	n^- epitaxial, thin	n^- substrate, medium	n^- substrate, thin
Additional layer	FS n epitaxial		FS n implanted
Emitter	p^+ substrate high efficient	p implanted low efficient	p implanted low efficient
Carrier life time	low by adjustment	high	high
			

Figure 1: Overview on different Trench IGBT concepts.

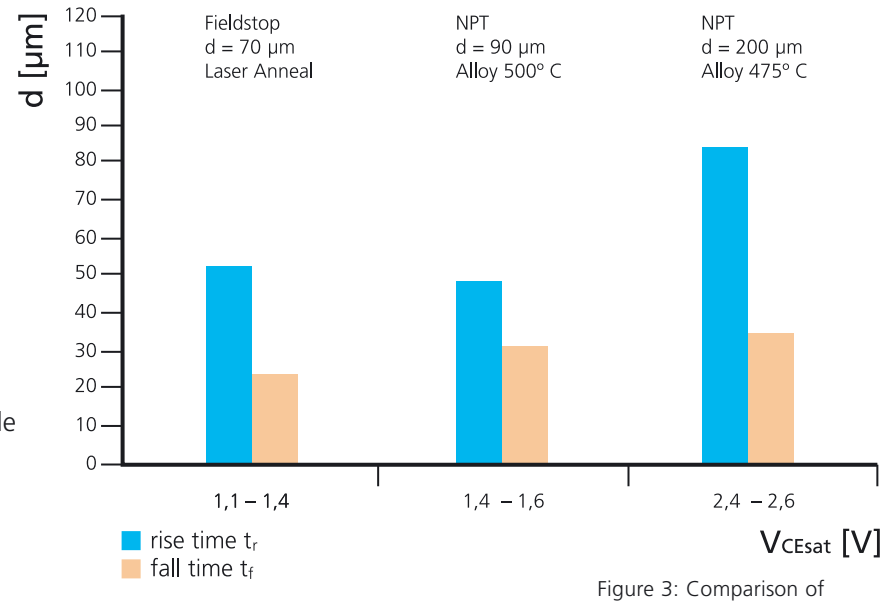


Figure 3: Comparison of electrical results for different Trench IGBTs.

The FS-layer is normally being formed by backside Phosphorous implantation with subsequent diffusion at a higher temperature. By this high temperature treatment it is not allowed to have the frontside metallisation already finalized due to the low melting temperature of Aluminum.

This implies that the frontside processes for metallisation and passivation as well as all backside processes have to be done with ultrathin substrates. For this purpose special techniques for ultrathin wafer handling are required with yield and hence cost impact.

In order to overcome the necessity of frontside processing with ultrathin wafers ISIT has developed a new approach for Fieldstop Trench IGBTs. In contrast to the diffused FS-layer as mentioned above a substrate with a n-type fieldstop concentration is used as illustrated in figure 2. The drift zone layer in the range of 50–60 µm is grown by epitaxy suitable for 600 V blocking voltage. After having finalized the frontside processing entirely the substrate is thinned down to a residual thickness of the FS-layer in the 5–10 µm range. The Emitter is then implanted with Boron and activated by laser annealing. Laser annaeling is carried out with a high energy XeCl laser at 308 nm with an energy density in the 2–4 J/cm² range. The advantage of laser annealing is the possibility of Emitter efficiency adjustment without any restriction on temperature impact on the frontside of the wafer. This is due to the fact that even in the case the backside Si is melted by laser exposure the high temperature will ease off over a few microns below 300 °C which keeps the wafer frontside cold.

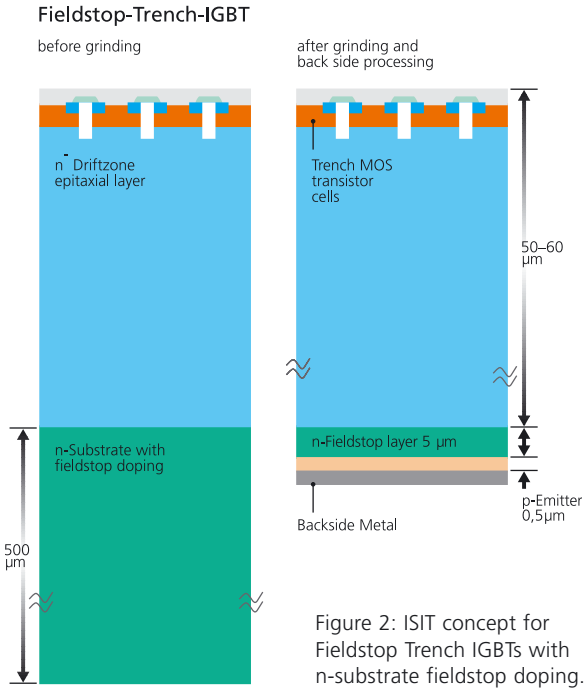


Figure 2: ISIT concept for Fieldstop Trench IGBTs with n-substrate fieldstop doping.

This kind of processing gives the opportunity of using a carrier concept for ultrathin wafers based on temporary bonding by use of a doubleside glueing thermal release tape. By this principle the IGBT wafers have to be temporarily bonded upside down on a carrier wafer after finish of the entire frontside wafer processing. All backside processes like grinding, etching, implantation, metallisation and laser anneal can be carried out with the same carrier concept for handling substrates in the 50 µm range.

First electrical characterisations have shown remarkable results with saturation voltages of about 1,1–1,3 V and a turn-off time in the 20 ns range shown in figure 3. With this new laser technique for backside Emitter annealing the trade-off optimisation between conducting and switching losses can be maintainted efficiently with further potential of performance improvement.

Ultrathin PowerMOS Devices

PowerMOS devices are preferential power switches for sub 100 V applications. The device is organized in millions of parallel transistor cells guiding the current from the front side to back side of the device. The transistor cells are controlled by Poly-Si Gate structures embedded in Si trenches. Comparable to highly integrated CMOS devices the cell density of PowerMOS transistors is increased with every new generation by geometry scaling. State of the art PowerMOS transistors reaching a cell density of 300 million cells per inch^2 with feature sizes of 0,4 µm for the trench gate electrodes. According to the PowerMOS roadmap it becomes clear that feature sizes of 0,25 µm will be reached in the near future with cell densities in the range of Giga per inch^2.

The most important performance parameter of a PowerMOS device is the On-state resistance R_{DSon}. The value of R_{DSon} depends on the maximum blocking voltage V_{BR} of the transistor and is increasing according to a $V_{BR}^{2,5}$ dependency. The main contributions to R_{DSon} are the serial resistances of the transitor driftzone R_{DZ}, the transistor channel R_{Ch} and the Si-substrate as shown schematicaly in figure 1.

The constribution of further resistances for contact, Source, and the accumulation zone are neglected. Since the drift zone has to support the blocking capability of the PowerMOS device the drift zone resistance R_{DZ} will rise with the blocking voltage. This is due to dopant concentration lowering and the increase of the drift zone thickness. The channel resistance R_{Ch} depends strongly on the cell density whereas the substrate resistance R_{Sub} increases with the substrate thickness.

According to those rules the lowest R_{DSon} can be achieved for low voltage PowerMOS devices with highest cell density and ultra thin Si-substrates. This exactly is the scaling strategy for PowerMOS devices fabricated by our industrial partner Vishay Siliconix Itzehoe.

With regard to new PowerMOS generations the feasibility of ultrathin substrate technology was investigated together with Vishay.

Therefore, the thinning process by wafer grinding as well as the handling of ultrathin Si-substrates are the most important topics which have been addressed. For the handling concept it was decided to use the so called temporary bonding based on a double side glueing thermal release

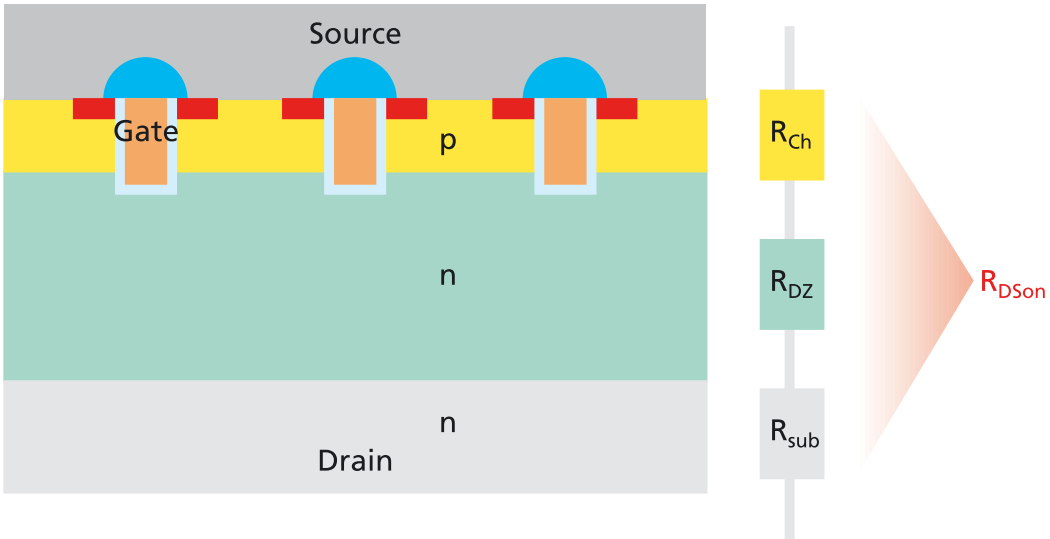


Figure 1: Schematic of a Trench-Gate PowerMOS device. The main contributing serial resistances R_{Ch}, R_{DZ} and R_{Sub} to the On-resistance R_{DSon} are shown.

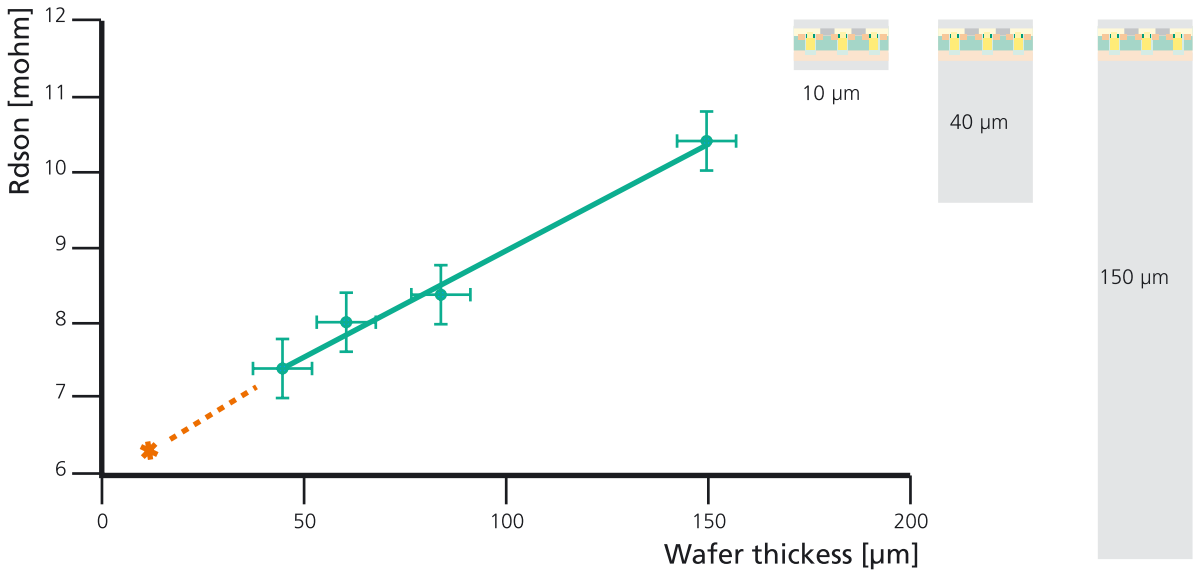
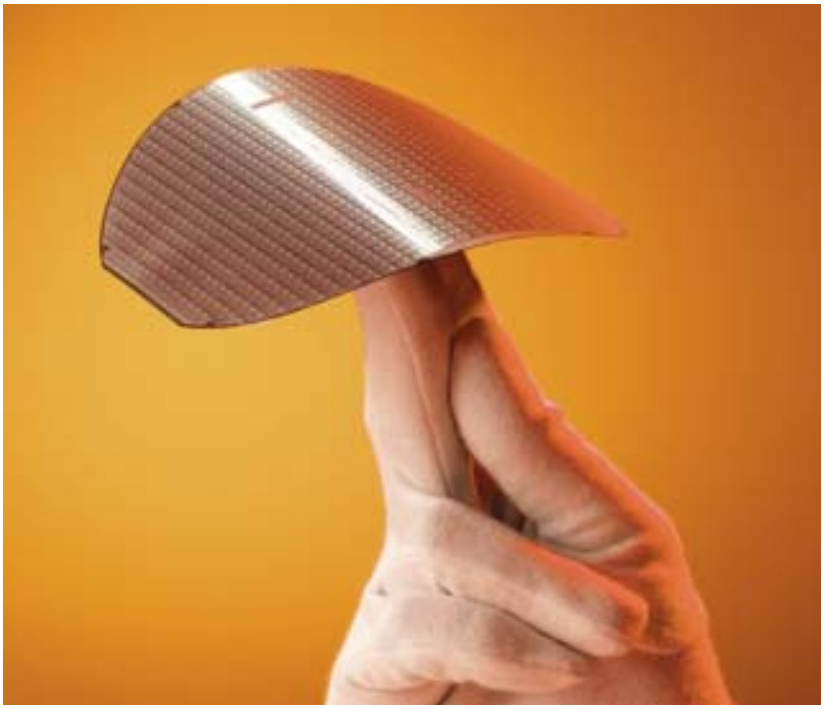


Figure 2: Dependence of On-resistance R_{DSon} vs substrate thickness for 30 V Trench PowerMOS devices.

tape. Using this concept the PowerMOS wafer is temporarily bonded up side down on a carrier wafer with the thermal release tape in between. This stack has been proven to be compatible for all back side processes such as grinding, stress release etching and metallisation.

State of the art 30 V PowerMOS devices were fabricated with substrate thicknesses down to 40 µm. The On-Resistance improvement of a 40 µm PowerMOS transistor compared to a 150 µm reference device was measured in the range of 30 %. As shown in figure 2 a linear dependency of R_{DSon} on substrate thickness can be observed.

It is expected that further substrate thinning down to 10–20 µm can be supported by this bonding techniques. A remaining substrate thickness of 10µm would result in 40 % R_{DSon} improvement compared to a 150 µm reference device.



Passive Components: High Precision Chip-Capacitors for GHz-Application

The demand on High Precision Capacitor (HPC) components for high frequency applications is growing with new generations of radio receiver and filter networks e.g. mobile phone/UMTS, GPS and VCO. At the Fraunhofer ISiT, HPC components have been developed and are now being fabricated for our industrial partner Vishay by the use of IC mass production technology. The new developed HPCs are combining an increased product performance with reduced dimensions and weight.
The capacitor is designed for upside down flip chip assembly on printed circuit boards or smart card applications. The device principle is shown in the cross sectional drawing of figure 1. High conductive silicon wafers are used as a basic material for HPC processing. At first the dielectric SiO_2 film is formed. Depending on the required capacitance value and the dielectric film thickness, a SiO_2 non-uniformity of less than 1 % can be realised. The film growth is the key process which assures the component to have a close capacitance tolerance of +- 1 %, which is excellent compared to competitive products with a tolerance spread of 5 % to 10 %. The top plate of the capacitor consists out of a 3 layer metal stack. The outer termination of the component is realised either by solder bumps or by gold termination. For moisture protection, the component surface is sealed up by passivation layers.

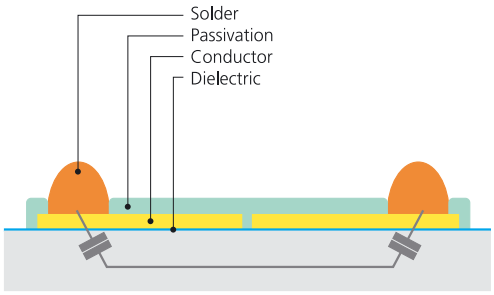


Figure 1: Cross sectional drawing of a chip capacitor with solder bumps.

It is useful to define a capacitance density C_F which is representing the capacitance value relating to the capacitance area. The capacitance area can not be increased, since the dimension for the components are fixed. The only way to increase the capacitance is to reduce the oxide thickness. The minimum possible oxide thickness for a certain voltage V_{max} is determined by the break through field strength E_{max} of the dielectric material. With the increasing quality of the dielectric material also E_{max} is enhanced. This allows the use of thinner dielectric film that results in an increase of the capacitance per unit area C_F. A capacitance density C_F of 0,58 nF/mm² can be realised for HPCs which is about 10 times the value determined for usual surface mounted devices (SMDs).

The HPC fabrication is covering the component size of 0603, 0402 and 0201. The components are available with a solder bump or gold termination. The gold termination is designed for

HPC
High Precision Capacitor
Copper (Cu) Termination or Gold (Au) Termination

0603	0402	0201
0.8 pF ... 1000 pF 6 V ... 25 V	0.1 pF ... 180 pF 6 V ... 25 V	0.1 pF ... 39 pF 6 V ... 50 V
uniformity: +/- 1% or 0.05 pF parasitic inductance: ~0.046 nH	uniformity: +/- 1% or 0.05 pF parasitic inductance: ~0.032 nH	uniformity: +/- 1% or 0.05 pF parasitic inductance: ~0.035 nH
Dimensions: W = 0.8 mm L = 1.60 mm	Dimensions: W = 0.51 mm L = 1.02 mm	Dimensions: W = 0.3 mm L = 0.61 mm
copper + solder: T = 0.56 mm	copper + solder: T = 0.40 mm gold wire bond: T = 0.18 mm	copper + solder: T = 0.23 mm gold wire bond: T = 0.18 mm

Figure 2: Survey of HPC components ranging from the component size 0603 to 0201. The dimensions of the components are displayed also, namely width (W), height (H) and thickness (T).

Figure 3: HPC components of different overall size, 0603 (left), 0402 (middle) and 0201 (right).

wire bonding applications e.g. in contactless chip-cards. The solder termination is best for printed circuit board (PCB) assembly. Depending on the required soldering process, the solder bumps can be lead free, according to the requirements of the EU, the USA ANSI norm and also to the RoHS Compliant (Restriction of the Use of Certain Hazardous Substances in electrical and Electronic Equipment). A general survey of the components with the key technical data is given in figure 2. The capacitor range and the voltage rating is shown. Pictures of some separated components with the size of 0603, 0402 and 0201 are shown in figure 3.

Depending on the component size the capacitance is ranging from 0.1 pF to 1000 pF with a voltage rating of 6 V to 25 V for 0402/0201 and a voltage rating of 6 V to 50 V for 0603 capacitances. It was proven that 0402-size components can handle high power levels of e.g. up to 88 watts with no change in capacitance value, no physical damage, and non-measurable difference between pre-test and post-test parameters. Precision RF capacitors like single-layer, low temperature, co-fired ceramic chip capacitors (LTCC) or single layer, thin film (TF) dielectric capacitors where recognised as the most stable types of chip capacitors with the highest self-resonant frequency (SRF) of about 3.5 GHz. For the new HPC components an SRF of more than 10 GHz was determined along with a high Q-value and minimised L-C parasitics. Very low inductive

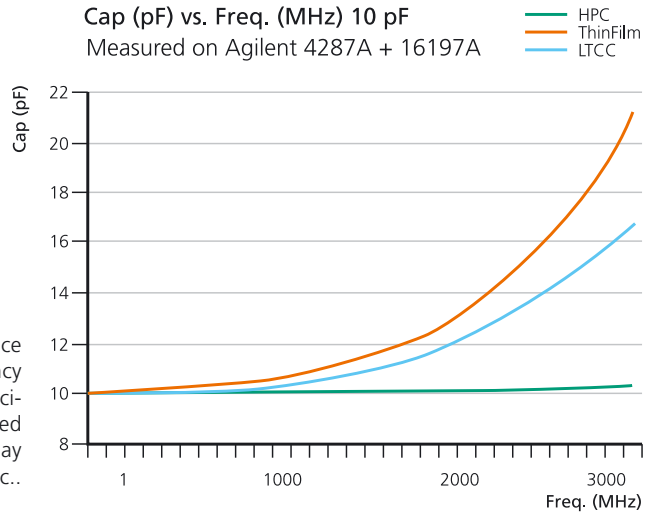


Figure 4: Capacitance change vs. frequency for 0402 HPC capacitors, measured at Vishay Intertechnology, Inc..

parasitics could be realised by the use of the special SMD component designs and the employing of a solder bump technique. Typically, the RF capacitance value of standard components is increasing with frequency due to parasitic inductance impact. As can be seen in figure 4 there is nearly no capacitor change with increasing frequency which is a specila advantage for this circuit design.

After finishing the processing, the silicon wafers are diced in order to get single components. Figure. 5 shows a silicon wafer with HPC components right after dicing. After separating the components from the dicing tape, they will be processed into tape and reel, ready for use.

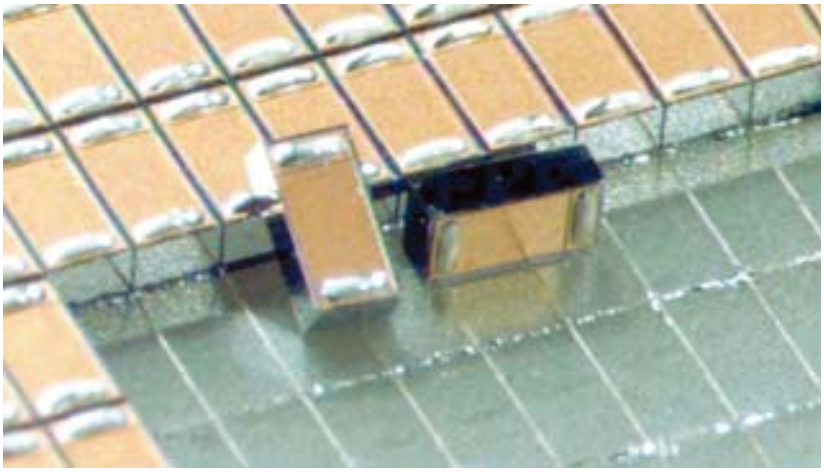


Figure 5:
0603 HPC components after separating.

Research Cooperation with Algeria, Semiconductor Processing in Algiers

The Centre for Development of Technology in Algeria, CDTA, located in Algiers is an important research institute for testing and design of electronic circuits. Starting with several visits from representatives of CDTA in Itzehoe a programme was discussed to allow CDTA an independent processing and development of silicon based semiconductors. As one result of the discussions the Algerian Government has decided to build a cleanroom of approx. 1000 m^2 area and to install a CMOS processing line in the new cleanroom laboratory. Build up of the cleanroom in Algiers next to the CDTA started beginning of 2005. Meissner & Wurst, Zander has been contracted as responsible partner for the cleanroom set-up. ISIT was choosen as technological partner for support in the design of the cleanroom and media supplies, selection of processing equipment and to transfer Know How and process parameters to allow installation of a 1 µm CMOS process in the new research lab of CDTA. Therefore, ISIT has prepared a documentation of a 1 µm CMOS process flow including design of several test structures to allow an evaluation and characterisation of the technological parameters for the process flow in Algiers. This documentation was presented during a workshop in Itzehoe and handed over to engineers of CDTA. ISIT has prepared a detailed time schedule for availability of necessary equipments and process modules to start an efficient process installation when the new cleanroom is finished. As part of this time schedule the engineers were identified that have to be available at various critical process sections to take over responsibility for silicon processing in Algiers. Documents were prepared for CDTA describing and defining all materials necessary for silicon processing including safety and material data sheets.

To make engineers of CDTA familiar with their future tasks and responsibilities in semiconductor processing a training schedule was created and groups of process engineers visited ISIT for a training course in their specific technical field. Three groups of engineers participated in training courses which include all for CMOS fabrication necessary process sections: The first group was teached in lithography and wet chemistry. There, the specific tasks as resist treatment and cleaning procedures were exercised. The exposure course was performed at the GCA 8000 stepper, which was supported by the company Professional-Maintenance. The second course included implantation, high temperature processes, diffusion and deposition, and dry etch. The final training

Figure 1: Model of the final complex of the
"Centre de Développement des Technologies Avancées" (CDTA).

was performed in thin film deposition, metal and PECVD, dicing and assembly, and process integration. There, the main issue was put on the understanding of the electrical characterisation of test structures and its correlation with technology related subjects.

All courses started with an introduction into working in a cleanroom environment and safety instructions for working in a laboratory. Subsequently, the specific subjects of the respective processes were practised. Process modules needed for the 1 µm CMOS process were introduced and discussed. For all technology areas the CDTA engineers have been trained by practical work at the production equipment at the ISIT cleanroom.

Additionally, CDTA asked for advise in organisation of material procurement, secure handling and storage of critical process materials and organisation of quality and safety measures. Therefore, an additional group of CDTA employees came to visit ISIT for two weeks to gain insights into the daily operations within a semiconductor line. Together with this group some members of the future facility maintenance group at CDTA were introduced into the facility service schedule at ISIT.

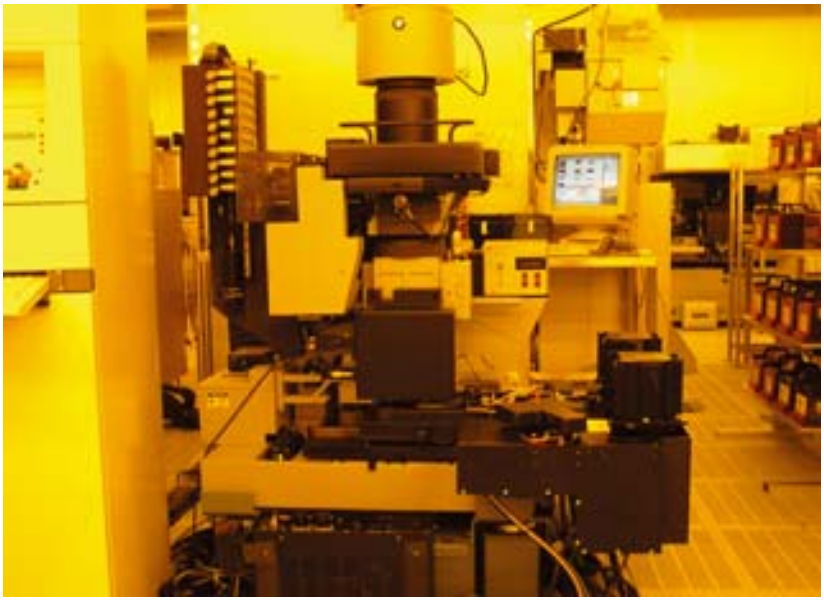


Figure 4: Exposure tool provided for the 1 µm CMOS line at CDTA.

After successful finalisation of these training programmes the next steps to install a CMOS line in Algiers will be

- start of operation of CDTA cleanroom,
- installation of equipment in Algiers,
- start of equipment operation.

When these project milestones have been met by CDTA process engineers ISIT will give further support to organise a complete process flow, leading to the first test chips to be manufactured at CDTA. In CDTA an experienced group for circuit design is working and using various foundry services to produce final circuits. Using the process parameters of their own 1µm CMOS process CDTA will be able to manufacture and evaluate its own independent technology.

Figure 2: Entrance of the in the year 1988 founded institute.

Figure 3: View onto the building site of the clean room.

Development of a Biowarfare Toxin Microarray

In the field of Fraunhofer ISIT`s electrical biochip technology and in close strategic partnership with eBiochip Systems and Diehl BGT Defence, one focus of application is the detection of biological warfare agents with fully automated, portable and fast devices. Next to the analysis of bacteria (e.g. plague, tularaemia); spores (e.g. anthrax) and viruses (e.g. smallpox) by DNA or RNA hybridisation techniques, the determination of protein based toxins by sandwich immunoassays is of special importance, since the ability for the sensitive and reliable determination of proteins on chip could be shown. In cooperation with the Armed Forces Scientific Institute for Protection Technologies – NBC-Protection in Munster, the automated and multiplexed detection of several biowarfare toxins was successfully established and further optimised in R & D projects.

Toxins of interest are Staphylococcal Enterotoxin B (SEB), Ricin and the Botulinus Neurotoxins (BoNTs) A, B and E. Ricin is a plant toxin, present in the seeds of Ricinus communis, and known from several attacks, e.g. the "umbrella attack" in England. Botulinus Toxins and SEB are bacterial products. Several subtypes of Botulinus Neurotoxins are known, with BoNT A being the most prevalent, inducing the disease Botulism from contaminated food and widely known as Botox in cosmetic surgery. Botulinus Neurotoxins are one of the most toxic substances. 1 nanogram BoNT A per kilogram body weight may be a lethal dose.

For detection, the principle of a sandwich assay (based on antigen-antibody-binding) is transferred to a silicon chip. In the first step, capture antibodies are spotted by piezoelectric nanospotting on the positions of the chip for immobilisation. Next, coated chips are inserted into a flow cell and ready for measurement. During the automated assay, the following immunochemical steps (figure 1) are carried out:

- Binding of the antigen (= toxin) at the respective capture antibodies
- Binding of an enzyme labelled detection antibody
- Substrate cleavage at enzyme-bound positions into an electrochemically active product
- Electrical read-out by redox-cycling of the electrochemically active product

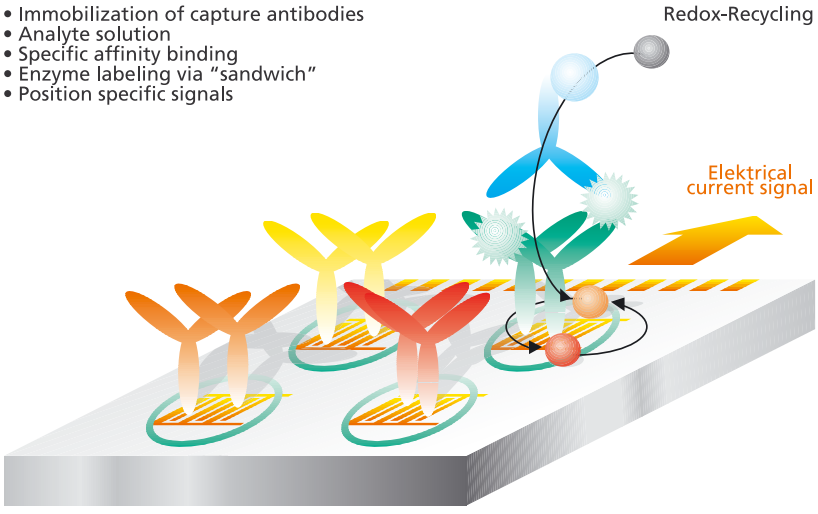


Figure 1: Scheme of a sandwich assay procedure.

A fully automated measurement cycle takes about 20 min. The electrical signal at each position is proportional to the amount of target toxin in the sample, which is determined by the amount of enzyme bound to each position. For the realisation of the toxin chip in array format, one of the most important steps is to find and combine appropriate antibodies, which on the one hand have a very strong antigen binding capacity and on the other side do not cross-react with other assay components (i.e. other antigens, antibodies or blocking components). Therefore, a wide screening of antibodies for each toxin had to be done, both in single and multiplexed assay formats. After selecting the antibodies, a toxin chip with a 16-position array design as shown in figure 2 was used. The chip includes 3 positions each for positive (binding the enzyme-conjugate) and negative (binding neither antigen nor enzyme-conjugate) internal controls and 2 positions each for the capture antibodies for the 5 different toxins.

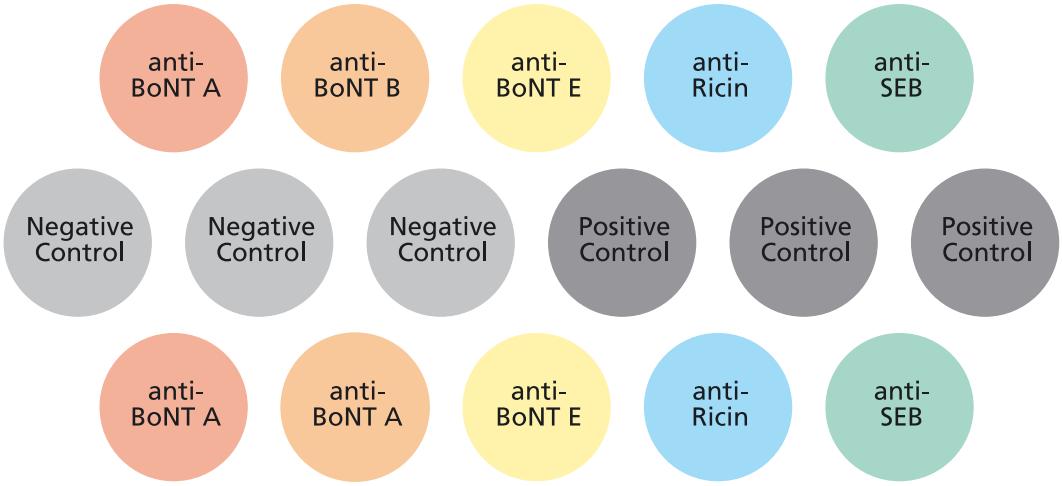


Figure 2: Array pattern for capture antibody layer of the toxin chip.

Results for measurements with only one toxin in the sample solution (figure 3) show the high selectivity of the sensor configuration. The sensitivity is different for each toxin. Those for SEB and ricin are comparable, but are at least a factor 10 higher than for the BoNTs. This reflects the different binding capacities of the antibodies for different assays.

The characterisation of an assay includes the determination of the limits of detection (LODs) for each toxin. The LODs (mean value of 3 measurements at one concentration minus standard deviation > 3 times standard deviation of the mean value of 3 measurements of the blank value) are:

- SEB: 0,3 ng/ml
- Ricin: 0,3 ng/ml
- BoNT A: 8 ng/ml
- BoNT B: 5 ng/ml
- BoNT E: 10 ng/ml

Studies with a spectrum of environmental and food matrices like soil, flour, milk, etc were started, indicating a broad application ability and robustness of the system.

The collaboration with the Armed Forces Scientific Institute for Protection Technologies – NBC-Protection in Munster will be continued during next year.

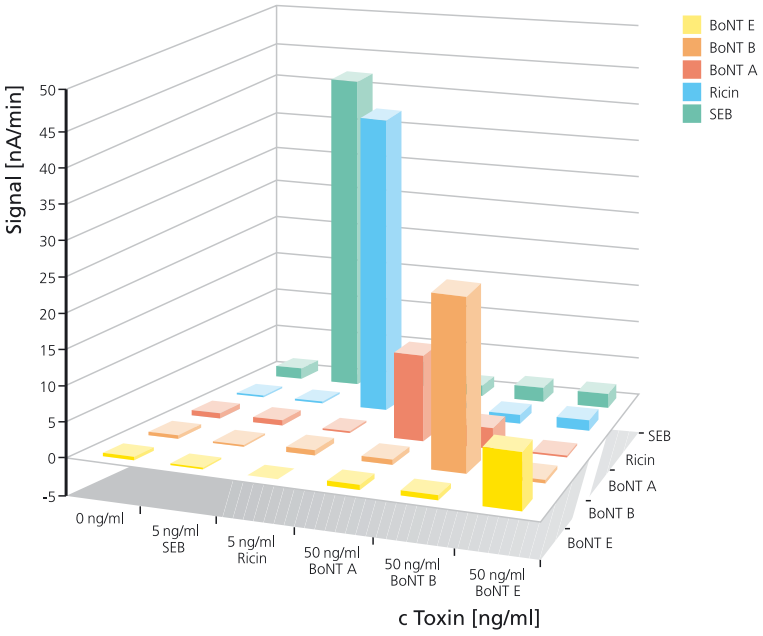


Figure 3: Signals of 6 measurements with one toxin per sample on the toxin array chip.

Representative Results of Work
Biotechnical Microsystems

New Analytical Systems with Electrical Biochips Developed in Cooperation with the Spin-off Company eBiochip Systems GmbH

The electrical biochip-technology is based on microarray biochips made with silicon-technology. The biochips, with 16 independent sensor positions, are modified with suitable bio-interfaces for the identification and quantitation of nucleic acids, proteins, and haptens. Together with the automated measurement devices, the biochips are the core components of the analytical systems.

The electrical biochips with sub-micrometer structures are designed, optimised, and produced in the industrial production-line at the Fraunhofer Institute for Silicon Technology (ISIT). eBiochip Systems GmbH, established in 2000 as a spin-off company of the Fraunhofer ISIT, develops, produces, and sells the complete analytical systems. These fully automatic miniaturised systems are for example used in DNA and antibody diagnostics, in pathogens and biowarfare agents detection as well as in food and environmental analysis.

One main field of activity was the development of the basis of technology for different device types. In cooperation with eBiochip Systems, the department of Biotechnical Microsystems develops special high sensitive multi-channel measurement electronics combined with fluidic systems for the automatic assays. A major component which allows simple and convenient operation of the processing system is the so-called "ChipStick" technology. This technology enables the biochips to be packaged in cartridges for inserting into analytical systems where all fluidic, electrical, and thermal connections are made via a simple lever mechanism. Various ChipsSticks are available for different application- or customer-specific capture molecules. Different capture molecules dispensed on the 16 independent positions of the chip allow the simultaneous detection of different targets in a single sample. The dispensing is done by a special Piezo-Plotter supported by image

Figure 1: Section of a silicon wafer with electrical biochips.

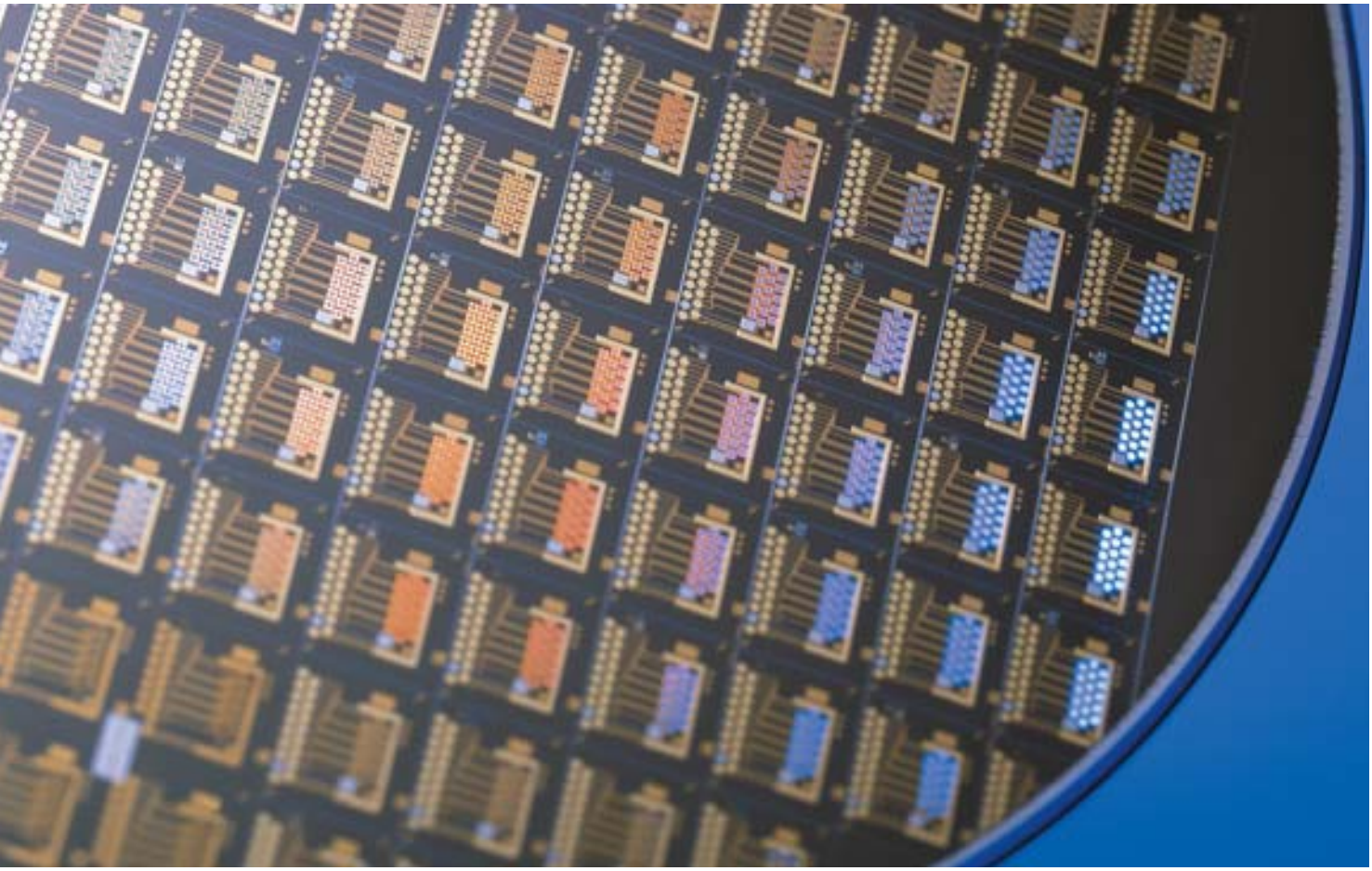


Figure 2: Insertion of the biochip packaged in a ChipStick.

Figure 3: Detail of the Piezo-Plotter dispensing bio-molecules on the array positons of the electrical biochips.

recognition capabilities. Other important developments of the automatic analytical systems are application-specific configurations and advanced analysis software for better usability. The combination of methods in bio-analytical chemistry with successful industrial methods of silicon- and microsystem-technology contributed to the development of flexible, portable analytical systems for a broad range of applications.

The new products offered by eBiochip Systems are: a universal device for research and development e. g. in the field of medical application called "eMicroLISA," a device for identifying biowarfare toxins and pathogens called "ePaTOX," and an educational training system for students and bio-technicians called the "Microarray Trainer."

eBiochip Systems and the Fraunhofer ISIT have also formed a close cooperation with DIEHL BGT Defence for the development and marketing of analytical systems for detecting biowarfare agents. In the same field of application, a collaboration with the "Armed Forces Scientific Institute for Protection Technologies – NBC Protection" for validation of the platform has been established. In the beginning of 2005 the project called "Nanoskalige elektrische Messverfahren für portable Analysesysteme niedermolekularer Verbindungen" supported by BMBF was completed. The concept for the development of portable analytical devices for the food analysis as proposed in the project was realised successfully. Also, in an ongoing project funded by the European Commission called eBIOSENSE ("Electrical Bio Sensor Arrays for Analyses of Harmful Micro Organisms and Microbial Toxins") nine participants are using the analytical system with electrical biochips as an assay development platform. In another EU-project titled IMPACT ("Innovative Measures for Protection against CBRN Terrorism") the analytical system was presented to participating members as a suitable bio-warfare detection platform.

Figure 4:
Different device types offered by eBiochip Systems GmbH.

Demonstration and Training Lead-Free Soldering for European Industry in Order to Promote Environmental Friendly Electronic Production

Mediating environmental awareness into electronics production

The new EU legislation on electronic waste stream and restriction of hazardous substances presents consequences for all parties involved in the electronics products supply chain: OEM manufacturer, contract assembly houses, equipment manufacturer, solder and flux manufacturer, PCB manufacturer, component manufacturer and distributor, and other consumables (gas/nitrogen, tooling) manufacturer, and, last not least, recycling companies and communal waste management.

The arising problems of this enforced law are especially harsh for SME assembly houses:

- Substantial cost factor due to necessary investments in new equipment
- Incomplete availability of RoHS and process compliant components
- Lack of compatibility of lead-free processing at higher temperature with existing device specifications
- Lack of experience with lead-free-specific inspection and repair routines
- Strong deficits of personnel skills regarding lead-free soldering
- Disruption of running commercial production during experimental introduction, feasibility tests and in-house training lead-free technologies not only in RoHS relevant, but also RoHS exempted applications.

Lead-free soldering means narrower process window

From July 1st, 2006 the use of lead containing solder in electronic assemblies is restricted by RoHS. The lead-free alloy system based on the ternary SnAgCu has by now been adapted by standardization as SAC305, i. e. 3.0 wt. % silver and 0.5 wt. % copper in a tin base. The melting point is between 217° C and 220° C, which is almost 40° C above the liquidus temperature of near eutectic tin-lead base alloys, e.g. SnPb36Ag2. Therefore, higher temperatures are needed for the solder process for melting the solder alloy and wetting the contact surfaces. This poses higher heat resistance requirements on the components, beside the need to adapt to RoHS compliant compositions with regard to lead free contact finish and compliant flame retardants. Unfortunately, the decomposition temperature of the industry standard polymer packages, plus the strong temperature dependence of the MSL (moisture sensitivity level) which classifies the danger of delamination during reflow soldering put a close upper limit to the process window. Revision C of J-STD-020 describes this in terms of time allowed above liquidus (60–150 s) and maximum temperature not to be exceeded (225/240° C, solder with lead; 245/250/260° C, lead free solder, for large/medium/small active components, respectively). Therefore, the process window is cut in half with regard to temperature tolerance, putting much more demands on process and equipment control. Thus, the process logistics have to be reviewed with regard to open times of components and work in progress. The personnel have to be trained accordingly, with regard to closer process control and monitoring.

External assistance in conversion to RoHS compliant products

The single process step of lead-free soldering in itself is already a manageable task, though to be mastered with these narrowed process tolerance. Assistance for this single step in electronics production is given e. g. by equipment manufacturers for individual users. The novel approach

now carried out at ISIT is the linkage of the complete process flow with the materials and design information available on environment-friendly technologies, including and beyond legislative boundaries. During the past five years, ISIT took part in several public and industry sponsored applied research projects with regard to fabrication and analysis of lead-free soldering processes. The new and innovative knowledge gained in these projects was essential for allowing ISIT to build up an environment-friendly process flow demonstration line by:

1) Choice of equipment (better energy / consumables management),
2) Set up and installation (focus on energy consumption in facility management),
3) Combination with process parameters (more efficient up-time use),
4) Operation of equipment in industry scale serial production, and
5) Hands-on training on a wide range of applications (personnel awareness of energy conservation).

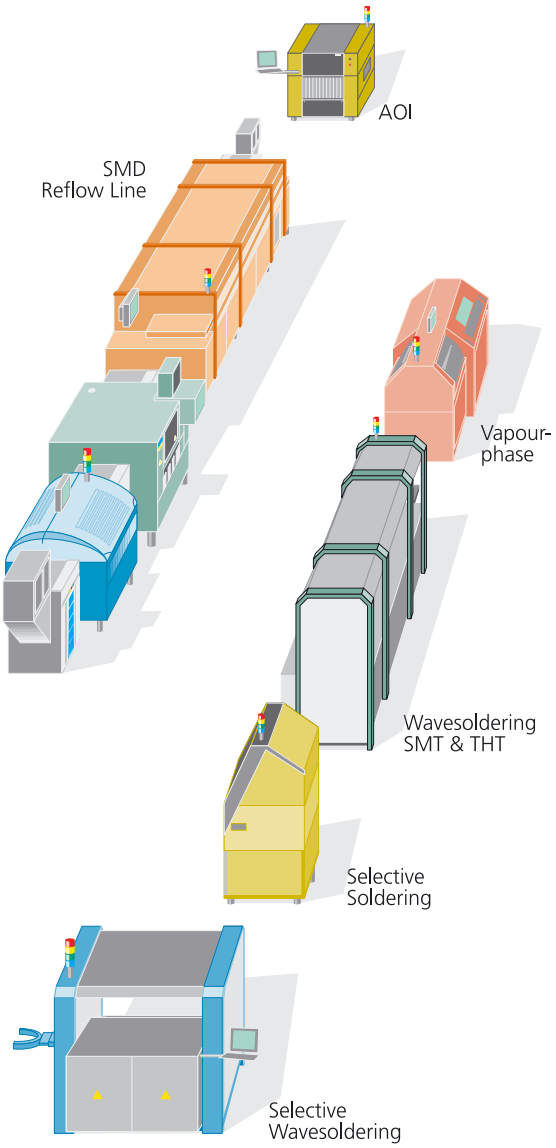


Figure 1: Schematic of the training line set-up.

The Life Environment LEADFREE project

In the framework of the EU Life Environment Program, the LEADFREE project solution installed and completed in December 2005 is a non-for-profit, pre-competitive European competence centre for demonstration, training and exercises to be used by European electronics manufacturers, who bring their own materials and test vehicles to practice with state-of-the-art lead-free soldering equipment, assisted by scientific engineering supervision and analysis including hands-on training.

The Life Environment LEADFREE project goes beyond the technology based projects in that these were examining different aspects of the industrial electronics assembly soldering methods, and now for the first time a complete demonstration line is to be run in accord with an integrated production policy (IPP) based on life cycle thinking. The project is innovative and unique by pioneering the application and translation of integrated production life cycle thinking into practice.

This enables ISIT to assist the client companies taking part in training and exercises in a product/customer specific way, while elucidating the EU environmental goals to the partaking candidates and demonstrating the ways to integrate environmental friendly electronics assembly with optimized material and process parameter selection. An innovation lies in the approach to mediate this environmental and product friendly approach also to single clients, thus presenting the possibility for SME to practice on their own discretion without the need to prior investment. The aim is to assist in evolution of sustaining technology in economically weak regions. In this way, the acceptance of environmental goals will be further increased, when it is demonstrated that environmental and economic goals do not exclude each other.

Representative Results of Work Module Integration

Technology provided

The LEADFREE demonstration and training line comprises the following technical elements physically implemented in the Basement Section of the Fraunhofer ISIT Clean Room:

A) Industrial LEADFREE surface mount assembly line suited for reflow and wave soldering (see figure 1).

B) Selective soldering process technologies featuring laser soldering, induction soldering, automated hot iron soldering, selective wave soldering (see figure 1).

C) Rework centre comprising several stations with innovative process equipment, such as mini wave, hot gas, and infrared soldering/de-soldering;

D) Inspection and analysis centre for quality control, including optical inspection, endoscope-optical inspection of hidden solder joints underneath components, AOI (Automated Optical Inspection), X-ray transmission radiography with micro focus resolution. SEM/EDX (Scanning Electron Microscope with energy dispersive element analysis), SAM (scanning acoustic microscope); needed for material qualification for lead-free soldering, and package decapsulation.

E) Special Training facilities and demonstration lab with work spaces for theoretical and practical training in mass production and manual soldering; best practice production and repair means higher first pass yield, increased reliability and less waste.

One focus of current investigations is on comparision of different main-stream solder alloys; this is achieved by exchangeable solder pots in the wave and the selective wave solder system, to provide three alternative alloys (see "case examples").

Practice and Training Concept

The quality and reliability group within ISIT has a decade history of seminars, and additional experience with certified IPC training. The institute, being a part of the Fraunhofer applied research society, partakes in education by offering and supervising student practical training and thesis projects; since five years, ISIT also educates microtechnology apprentices, establishing an intensive cooperation with the regional vocational school. Thus, the institute has established a holistic view on innovation and integration of new technologies from semiconductor via microsystem to electronics assembly fabrication specs. The training concept evolved from this approach is shown in figure 2, which will be explained in more detail in the following.

Currently, there is no education leading to a professional degree in either design or production of electronic assemblies in Germany. The need for confound education in this field is recognized. A first approach is the establishment of professional education on a craftsmanship level, namely microtechnology apprenticeship, carried out in various companies and institutes, accompanied by required learning sessions at vocational schools. As this education is to a great extent technology based, a follow-up program is being developed and tested to train and educate personnel on a technician level in this same field of microtechnologies. The action fields of this education are stated by RBZ Itzehoe (regional education center), the education to begin in fall 2006. Within the LEADFREE project, ISIT has now developed a practical training concept based on the technical action fields, to complement the RBZ education with the appropriate practical training on industrial production scale equipment. This enables even SME companies to qualify their personnel in a training-on-the-job concept for a technician level professional degree. The program further assists the companies to fulfill the new European environmental requirements by training modules which show how to integrate economy and ecology. Special focus is laid on resource management, to show basically that the best way of environment protection is by material and energy conservation.

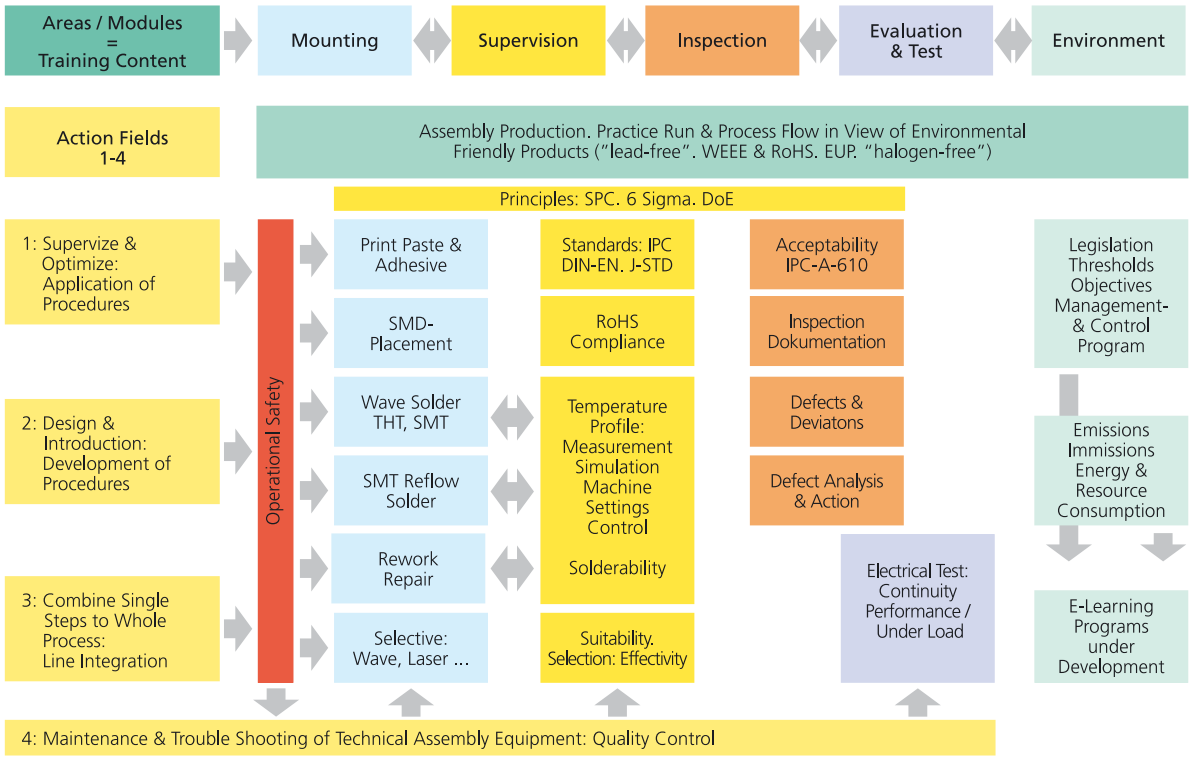


Figure 2: Schematic of the modular training concept.

Action fields 1 and 2 (figure 2) are a two level approach to the individual process steps, which are shown in the blue boxes. The first level ("supervise and optimize") teaches handling and application of materials and other consumables on given equipment on test assemblies. The second level ("design & introduction") teaches how to select and evaluate materials and equipment to improve yield or performance, and how to improve matching equipment, materials, and assembly. Action field 3 ("line integration") teaches how to combine single steps to a whole process. The respective and necessary details of these action fields are shown in the yellow (process requirements, process control) and amber boxes (end item evaluation); each box resembles a practical module with a duration equivalent of 20 h. This makes up for e.g. 120 h of process step practice on level 1 plus the same for level 2 (six modules on two levels). There is some planned redundancy by modules such as temperature profiling, which is applied in the soldering modules, but will be trained in-depth in a separate module, to understand the equipment, temperature calibration and more. Principles, such as SPC, 6-sigma, DoE (statistical process control, 6-sigma concept, design of experiment) are trained on live samples, again to complement theory taught at the college. Electrical test is a separate box and will be offered more in the sense of trouble shooting on machines and assemblies, because issues like In-Circuit-Test are taken to be part of product development and design rather than production. The modules on environmental issues will be loaded with responsibility information, such as legal requirements, combining environment, safety and health protection. The scope is saving materials, time and money, the training integrates process and product control management in line with required quality and environment management systems. This part will be further developed to become part of an "E-Learning" program offered as an output of the Life-LEAD-FREE project.

Representative Results of Work Module Integration

Integration of environment conscious process and quality analysis training for industrial users

A key goal of this training program is that each of the listed headlines presents a stand-alone training module which can be used by any industrial user. As a critical requirement for their success, the participant companies are offered hands on support and training on the complete demonstration fab line, equipped with innovative technologies for industrial scale soldering of components on printed circuit boards. LEADFREE helps reduce the environmental impact of electronic goods material selection, production, and waste stream, supporting implementation of the new relevant EU RoHS and WEEE directives and environmental policy strategic goals as expressed in the EuP directive. Each module will be offered at least once a year, depending on demand, and can be booked according to described prerequisites. Each user should estimate his level for the process modules, but can enter in any of the other modules to gain certification based on tasks and requirements described for each module. A well-known example of this type of program is the IPC-A-610 training on acceptability of electronic assemblies, which is offered as one module in the course of this curriculum.

The program is developed in cooperation with the vocational school, with equipment manufacturers, a regional industry circle concerned with soldering issues (Hamburger Lötzirkel), and with the FED (Fachverband Elektronik-Design) as a society representing SMEs from electronic design and assembly.

Case Examples

The background for the establishment of the Life LEADFREE training line was laid by several joint projects, some with public funding in cooperation with other research institute partners. At the same time, cooperation on a European level was founded by participation first in the EUREKA LEADFREE project led by EMPA (Eidgenössische Materialforschungs- und Prüfanstalt), followed by associated membership in ELFNET (European Lead-Free Network), both of which do not provide won funding, but allowed for exchange of information and wide collection of requirements for the action now achieved by set-up of the training line and the associated program. The first projects performed around the millennium turn were on different aspects of lead-free technology. They were

- Lead-free mounting of 0201 components, and effects of repair soldering on the lead-free solder joints.
- Process parameters and reliability for reflow with Sn-3.8Ag-0.7Cu and wave soldering with Sn-0.7Cu
- Effect of solder paste and temperature profile selection on voiding in BGA solder joints
- Effects of underfiller on the thermal cycling reliability of BGA and CSP assemblies
- Assembly of the future – area array and lead-free soldering; an evaluation of process and materials.

Present projects are concerned with evaluation of joint embrittlement soldered on ENIG surface

a) gull wing lead thickness 200 µm before, 180 µm after soldering.

b) copper pad thickness 35 µm before, 25 µm after soldering.

Figure 3: Copper leaching after double wave; Sn-3.5 % Ag at 265° C, low residue alcoholic no-clean flux.

a) soldering in air.

b) nitrogen atmosphere (ca. 60 ppm residual oxigen).

Figure 4: Effect of atmosphere on bridging; Sn-3.5 % Ag at 265° C, low residue alcoholic no-clean flux.

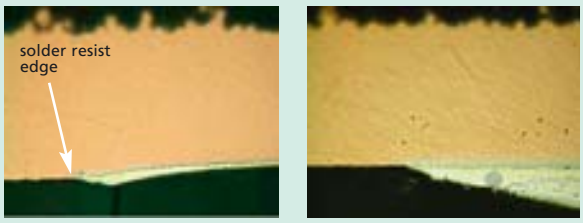


Figure 5: Effect of solder alloy on copper leaching; soldering at 255 °C, low residue no-clean flux.

a) Sn-0.7 %Cu; insert showing leaching structure.

b) Sn-0,7 %Cu-0,05 %Ni.

(electroless nickel / immersion gold), whiskering of tin finished contact surfaces – cause, mitigation practices, testing – and impact of voiding on the reliability of lead-free solder joints. Within the framework of EUREKA LEADFREE and Assembly of the future, several industry-financed projects were performed to focus on those issues which were of joint interest, but difficult to attain by one company alone.

Key examples are three consecutive projects on wave soldering

Solder tests were performed in mixed technology (SMT & THT components) first on a double layer, second on a multilayer with wave soldering only, and third on a multilayer test board laid out for reflow + wave soldering. It was found that 265 °C solder pot temperature was rather high, as copper leaching was as much as ten micrometer using a tin-silver solder alloy (figures 3 a and b). Further, at this temperature the flux activation was lost after the first wave, and it was necessary to solder in nitrogen atmosphere in order to avoid excessive bridging (figures 4 a and b).

The effect of nickel content on copper leaching

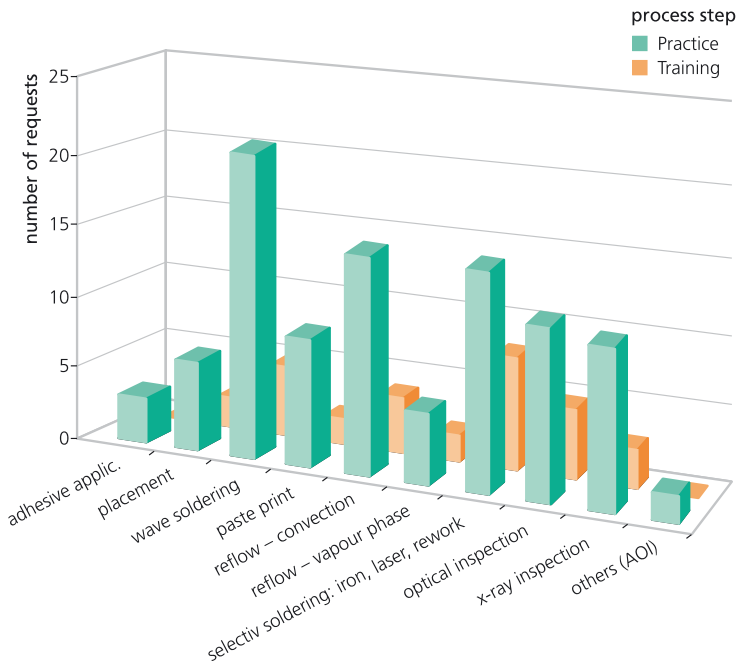
Figure 5 shows a microsection through copper pads after one pass over the double wave (soldering in nitrogen atmosphere). The average copper thickness is ca. 43 µm. With SnCu, copper leaching amounts to 3–4 µm from the surface (figure 5a), and the IP (intermetallic Cu-Sn phase layer) thickness is less than 1 µm. Using SnCuNi, the IP layer thickness is 2–3 µm, part of it reaching into the copper, part extending above the original copper surface, i. e. there is no measurable copper leaching (figure 5b).

Survey of the demand for centralized practice and training equipment

The wave solder experiments mentioned above were mostly performed at the site of and with assistance by solder equipment manufacturers. During the second set of experiments, a questionnaire was sent out to 40 members of the regional solder circle, to query the demand for equipment available for further investigations on lead-free soldering. From the 30 questionnaires returned, it could be deduced that there was a definite demand, and that the highest interest was in wave soldering; this is understandable, as this equipment is not easily reconfigured to switch between SnPb and lead-free soldering, especially as there are different alternative lead-free alloys. But also the other soldering techniques, namely convection reflow, and selective soldering.

This led finally to the Life Environment LEADFREE project proposal, culminating in the equipment set-up shown in figure 1. ISIT offers its clients use of the equipment with expert assistance for process and quality analysis. The contact can be made personally or via internet, see www.life-leadfree.de. Registered users can view the booking status of the line equipment, and can send their request via e-mail directly from the browser environment. The web pages provide information on the technical details and the boundary conditions on how to use the training line, and the availability of group training and the classical solder seminars held by Fraunhofer ISIT at Itzehoe.

Figure 6: Results of a potential user query showing demand for manufacturing and quality analysis practice opportunity.



Representative Results of Work Module Integration

Failure Analysis of Electronic and Microelectronic Components with a New Automatic Target Preparation System

Introduction

Electronic and microelectronic assemblies are complex material composites. The materials used are quite different in their chemical composition, their crystallographic structure and their microstructure. Of technical importance for the qualification of the components are interfaces, grain boundaries and phase boundaries as well as heterogeneous precipitations. Imaging and analysis of the microstructure is a prerequisite to estimate the quality of an assembly. Further criteria of qualification, from a metallographic point of view, are inclusions, contaminations, voids, cracks, holes, as well the evaluation of contours, e.g. the wetting angle of a soft solder connection.

In order to reach an excellent specimen surface, the samples have been prepared by hand up to the present day. So far only very experienced technicians have been able to work on difficult tasks such as thin wire bonds within intelligent chip modules. Another possibility is semi-automatic target preparation. The problem of both methods is that the specimen is in danger to be ground beyond the target layer and thus to be lost irretrievably, especially aiming at microscopic interior structures within complex electronic modules.

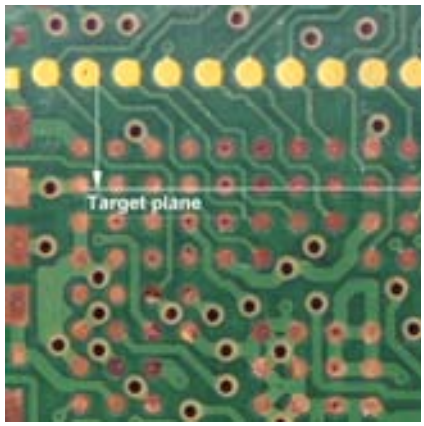


Figure 2: Printed Circuit Board with visible target, a row of microvias.

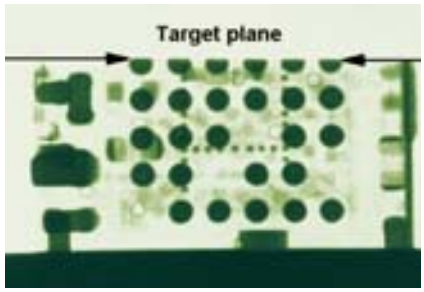
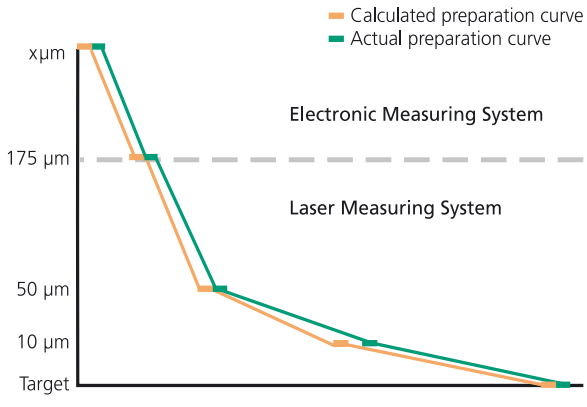


Figure 3: Radiographic image of hidden target, a row of solder balls on a CSP-component.

Based on the requirements regarding target, reproducibility, and specimen surface quality, an automatic system for controlled material removal and target preparation has been developed. The tool is for the metallographic failure analysis for electronics, and provides an accuracy of 5 µm. Fraunhofer ISiT has been able to obtain good results by running target preparation processes on the machine and has developed corresponding preparation methods.

Figure1: Overview of the Target Preparation System. Left side: Micropolishing System. Right side: Console for real-time alignment and measurement inside x- ray for hidden targets.

Figure 4: Electronic and Laser measuring systems.



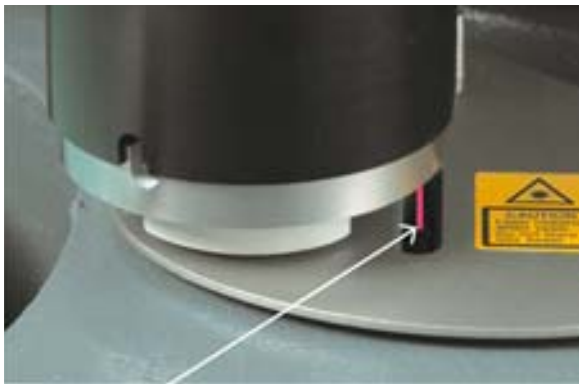


Figure 5: Laser measuring system.

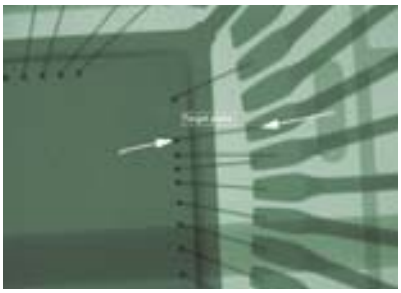


Figure 6: Real-time target alignment and measuring using x-ray and special set-up station.

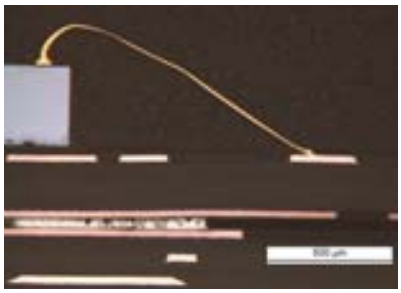


Figure 7: The entire length of the 20µm gold wire is visible in the cross section.

Description of the Preperation System
For automatically controlled material removal and preparation, the new tool offers alignment and measuring of the sample prior to the preparation. Cross sections of mounted and unmounted samples can be ground and polished to visible and hidden targets. A laser measuring system assures an accuracy of ± 5 µm and the removal rate is automatically calculated during the preparation process (figure 1).

Alignment and measuring can either be video based by a microscope for samples with a visible target (figure 2), or X-ray based for samples with a hidden target (figure 3). The new tool then calculates the total amount of material to be removed, starts preparation, and automatically stops the plane grinding step at a fixed distance from the final target plane of 175 µm.

At this point, a high precision measuring system takes control, and the following steps will take the preparation towards the target with breaks, as shown in figure 3, of preset, user-definable positions, e.g. 50 µm and 10 µm. The new tool automatically controls material removal by two separate measuring systems. Removal during grinding steps is controlled by an electronic measuring system, which continuously measures the distance to target.

In this fashion, the major part of the target distance is covered as quickly as possible. 175 µm from the target, a laser measuring system takes over. The system uses a relative measuring technique (figure 4). To achieve reliable measuring, the specimen is cleaned in two internal cleaning stations before moving to the laser measuring station. The use of laser measuring gives the system an accuracy of ± 5 µm (figure 5).

Preparation Method
Before starting the preparation, the sample is fixed with a special adhesive to a cross section jig, sample chair. The sample chair is then clamped into the sample holder and aligned and measured with X-ray in real time (figure 6).

Measured data is transmitted to the preparation system, and the sample holder positioned in the sample mover of the polishing machine. Before preparation starts, the sample height is measured and the removal time calculated for each of the steps. Table 1 describes the process summary and the polishing method of six samples with 20 µm gold wire bonds. The polishing process is interrupted according to predefined polishing times in order to allow a periodical laser measurement of

Figure 8: Wedge side of the wire.

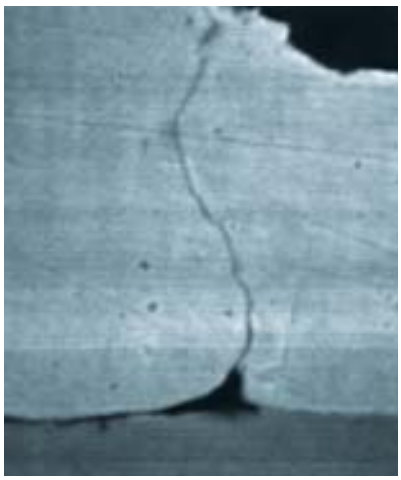


Figure 9: SEM image of wedge bond with crack.

Representative Results of Work Module Integration

Sample	1	2	3	4	5	6
Polishing/Grinding media	removal [µm]	removal [µm]	removal [µm]	removal [µm]	removal [µm]	removal [µm]
SiC#800	1691	1653	1697	1622	1677	1682
SiC#1200	261	260	256	254	253	255
MD- SAT 9µ	19	15	12	28	26	22
MD-Dur 3µ	2 min	2 min	2 min	2 min	2 min	2 min
OP-Chem 0.25µ	0.5 min	0.5 min	0.5 min	0.5 min	0.5 min	0.5 min
Target value	1971	1926	1965	1898	1958	1961
Distance to target	2	-2	0	-4	2	2
Time	34 min	34 min	35 min	36 min	31 min	32 min

Table 1: Process summary of wire bond preparation.

Step	1	2	3	4	5
Surface	MD-Fuga	MD-Fuga	MD-SAT	MD-Dur	MD-Chem
Abrasive	SiC	SiC	Diamond	Diamond	OP-S
Grit/grain size	800	1200	9 µm	3 µm	0.25 µm
Lubricant	Water	Water			
RPM	300/150	300/150	300/150	150/150	150/150
Force	30 N	30 N	25 N	15 N	15 N
Time	Dependant on the sample material and its grinding behavior			2 min	0.5 min
Removal	Target	250 µm	20 µm		

Table 2: Optimized preparation parameters.

the sample. The laser measurement allows an exact observation and control of the alignment to ensure that the targets will be reached exactly as intended.

The automatic preparation permits high precision as shown in figure 7, 8 and 9. The 20 µm bonding wire is visible along the complete length (figure 7) and also a crack on the wedge side is documented (figure 9).

Evaluation of the Equipment

The target surface quality depends on various factors:

- Grinding/polishing media
- Polishing time and force
- Mounting

It is essential to apply the correct pressure force and to choose the right polishing cloths and suspensions. It is recommended to use the diamond suspensions which exactly match the polishing cloths. The set removal time results from the depth of deformation, caused by the grinding or polishing media.

For instance, in Step 2 (grinding with silicon carbide paper) it is recommended to preset the total removal at 250 µm. Table 2 shows the optimized preparation parameters. It is also essential to choose the correct mounting material.

For filigree structures, such as microvias in printed circuit boards or thin wire bonds, epoxy resins fill and adheres better to cracks and holes. The preparation results achieved are in line with the specifications of the tool manufacturer, i.e. the required precision of ± 5 µm will indeed be achieved. However to get such exact results it is essential to work accurately.

The following factors can cause deviation in target measurement:

- Wet sample and/or reference plane by laser measuring after cleaning process
- Person doing the initial measurement did not work accurately

Examples of preparation

The evaluation of electronic devices (quality of production and reliability) offers a number of samples for the metallographic target preparation system. The following images show typical objects of examination in the analysis of microstructures and materials in the electronics packaging industry with brief comments.

Figure 10: Status quo of the braided wire before dipping 1000x (micro section).

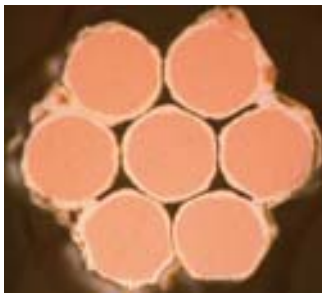


Figure 11: SnAgCu 0.5 – strong dissolution 1000x.

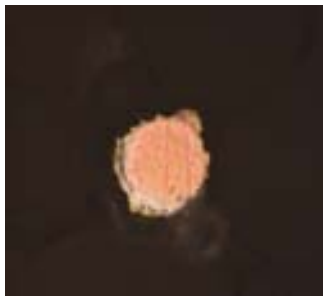
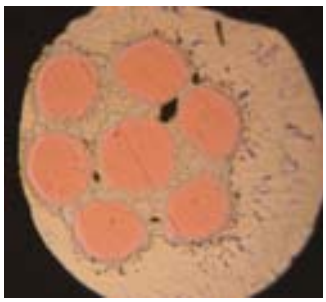


Figure 12: SnAgCu 1.3 – lower dissolution rate because of copper saturation in solder alloy 1000x.



Dissolution

Dissolution is necessary for forming the initial intermetallic compounds in solder joints. Dissolution is the metallurgical change that takes place as solid materials melt into liquid materials. Dissolution of metal substrates and their protective metal coatings occurs during soldering operations including wave soldering operations, reflow, rework, and repair.

Precious metal surface finishes (i.e. silver, gold, and palladium) and base substrates (copper and nickel) are involved in the dissolution process. The rate of dissolution depends upon the composition of the base metal and solder, cleanliness, and solders velocity. The dissolution rate also varies exponentially with temperature.

The sample (figure 10 and figure 12) shows a thin braided wire with 7 cores dipped in molten lead free solder three times at 260 °C. Figure 10 shows the state before dipping; and figure 11 shows the strong dissolution of the copper wire in SnAgCu 0.5 solder. There is only one core left. The other six cores are dissolved. Cause for this strong dissolution is the low copper content inside the solder alloy. With the saturation of copper in the solder alloy (use of SnAgCu 1.3, figure 12) the dissolution will be reduced significantly. For the usage of a lead free solder alloy this fact should be noted.

Whisker growth

Tin whiskers are growth structures of small diameter (~1 µm) that develop out of pure tin plated surfaces. The growth can cause short circuits or functional damage to another part of the product.

With the accuracy of the tested preparation method it was possible to display a single whisker in the microsection (figure 13 and figure 14).

Tin whiskers can form in a wide range of shapes, length and sizes. Whisker growth is attributed to the driving force to relieve internal stress that is created during the coating process, and during bending, forming and similar mechanical actions on tin plated structures.

Conclusions

The new automatic preparation system evaluated in this work can be used for the metallographic failure analysis on electric and microelectronic components. The desired preparation layers were achieved precisely and reproducibly with several specimens of the same kind. By hand, only experienced and skilled technicians can prepare such specimens of good quality, and still it is difficult and time consuming. Typically the specimens are at risk of being ground beyond the target and lost for further investigations.

The automatic preparation system, however, allows the preparation of critical samples within a short time, with high precision and with a excellent reproducibility.

Figure 13: SEM image of a galvanic pure tin surface with different shapes of whiskers.

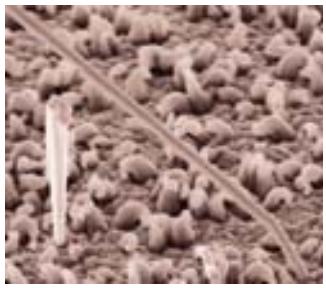
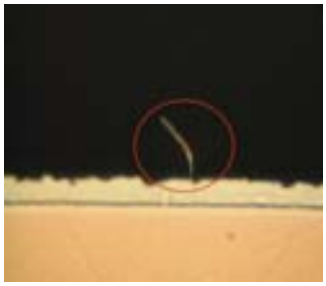


Figure 14: Microsection of tin layer with grown whisker (preparation plane measured with optical measuring station).



Material Optimization for Lead-Free Soldering of Fine-Pitch Flip-Chip Applications with Thinned Dies

Due to environmental and health considerations the European Parliament has passed a directive entitled "Restrictions on the use of Hazardous Substances" (RoHS). This Directive prohibits for many applications the usage of some precarious elements in electrical/electronic equipment sold after July 1, 2006. One of the banned elements is lead (Pb) which in the past was used as part of the common eutectic Tin-Lead (SnPb) solder. Due to the RoHS directive the tin-lead solder is replaced by lead-free alloys containing a very high tin content. The processing of the new composition requires increased soldering temperatures which are no longer compatible with the previous flux compositions. Since a good flux selection is crucial for the yield of fine-pitch flip-chip applications we have evaluated a selection of tacky fluxes from different suppliers. The results for daisy-chain flip-chips designed and fabricated at ISIT are shown in the table.

Flux	Yield on rigid substrates	Yield on flex substrates
A	96%	82%
B	98%	99%
C	91%	99%
D	28%	96%

There was only one flux which performs well on flex and rigid substrates whereas two fluxes show a very different behavior depending on the substrate material. We have also evaluated the influence of the substrate metallization. Due to the high activation of the used fluxes no significant difference between tin (Sn) and electroless nickel immersion gold (ENIG) finish has been observed.

The next optimization step was the evaluation of selected underfill materials. For flip-chip applications typically an epoxy glue is used to seal the gap between the chip and the substrate. This sealing provides protection against humidity or other corrosive substances as well as a dramatic increase of the mechanical bond strength. This so called underfill material typically is applied with a needle dispenser after the reflow soldering of the chips. Since the bond strength and the flow behavior of the underfill

flux **A**
underfill material **a**

flux **B**
underfill material **a**

flux **A**
underfill material **b**

Figure 1:
Investigation of voids with ultrasonic microscopy for different combinations of flux and underfill material.

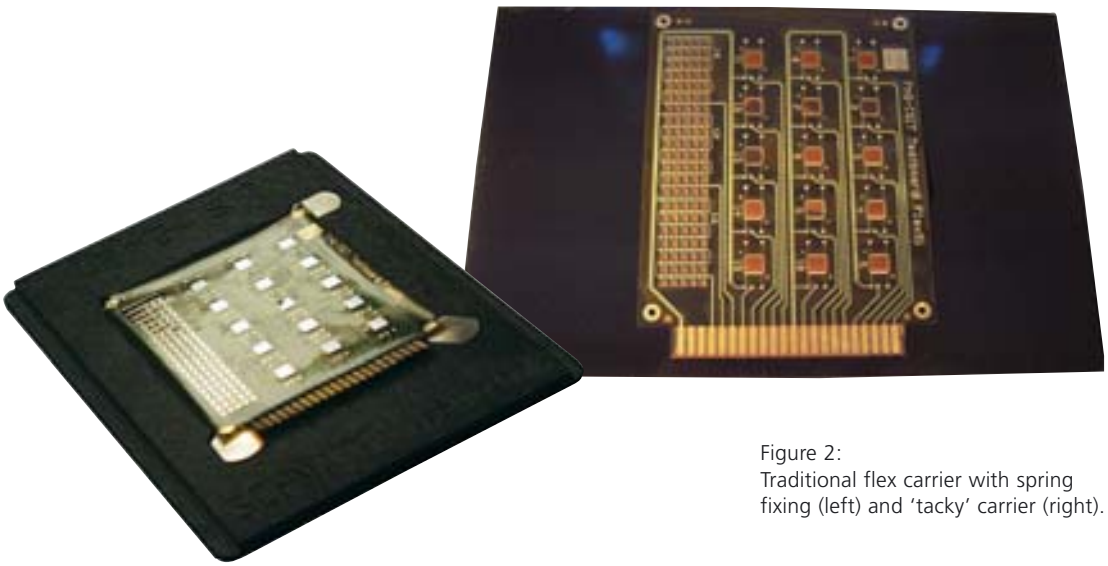


Figure 2:
Traditional flex carrier with spring fixing (left) and 'tacky' carrier (right).

material depend on the flux residues it is necessary to optimize the material selection with regard to the chosen flux.

Three examples of flux underfill combinations on a rigid substrate are shown in the figure 1 which has been taken by ultrasonic microscopy. The combination of flux 'A' with underfill material 'a' results in voids which could be a reliability problem. The same flux and underfill material combined with an other partner don't show any void. Furthermore no voids have been observed for any flux underfill combination on the flex substrates! The reliability of the assembled devices has been tested with an accelerated aging test based on water damp and heat. Independent of the voiding problem described above no early failures have been observed for any combination.

As a last optimization step the influence of the die thickness has been evaluated. Within the experiments we have used a die thickness of 680 µm (first experiments), 180 µm (most experiments), and 80 µm (some additional tests). Based on our experiences from the FLEXSI and FLIBUSI project the assembly of the thinned dies was trouble-free. Due to the reduced mass of the thinned chips we have initially observed lost dies during the reflow process. Since a reduction of the ventilation is not recommended for an oxygen-free reflow process a shielding technique was developed which solves the problem completely. At the end we achieved a very good yield which was independent of the die thickness.

Handling concept for arbitrary flex substrates

The handling of flex substrates requires a carrier concept for the die placement and reflow soldering. Traditionally springs are used to stretch the substrates on a rigid carrier (figure 1). Due to the mechanical nature of the fixation the design of the carrier has to be adapted to the geometry of the flex substrate thus a new substrate design requires new carrier boards.

To overcome these limitations a new carrier concept based on 'tacky' aluminium and G11 carriers has been evaluated (figure 2). For thin but rigid substrates both carrier materials have performed very well. For real flex substrates however the bending of the G11 carrier during the reflow process caused many connection failures. The aluminium on the other hand performed well for flex and rigid substrates.

Rechargeable Batteries for Hearing Aids

Battery powered electronic medical devices are often operated by non rechargeable batteries. For economical and environmental reasons a replacement by rechargeable batteries is a priority objective. Another important objective is an improved user-friendliness.

Specific requirements regarding the electrical performance and design of the energy storage unit often call for solutions which can not be provided by of-the-shelf secondary batteries. In the field of hearing aids for example highly different profiles of the accumulator – depending on the particular application – have to be met (figure 1).

- Implantable rechargeable batteries ("IMP") for cochlear hearing aids require primarily excellent long term reliability in combination with very high cycle stability while highest energy density is not of major importance.
- In external hearing-aids high energy content of the very small sized battery is a primary objective. Lifetime of the rechargeable battery ("EXT") is not that critical because replacement of the battery is not that difficult.

According to these specific criteria a dedicated battery development project can basically be separated into two parts:

- Development of a suitable battery chemistry and layout
- Development of an appropriate housing concept

In the framework of the European project HARPOS (Hearing Aids with Rechargeable Power Supply) it could be demonstrated that the rechargeable lithium-polymer-battery-system developed at ISIT can be matched to these very specific demands:

Implantable hearing aids

Contrary to current cochlear implant solutions with in parts external components future systems (hearing aid and the battery) should be fully implantable. This very challenging alternative is favourable in terms of handling, reliability and cosmetic aspects. The housing technology has been developed in close cooperation with industrial partners.

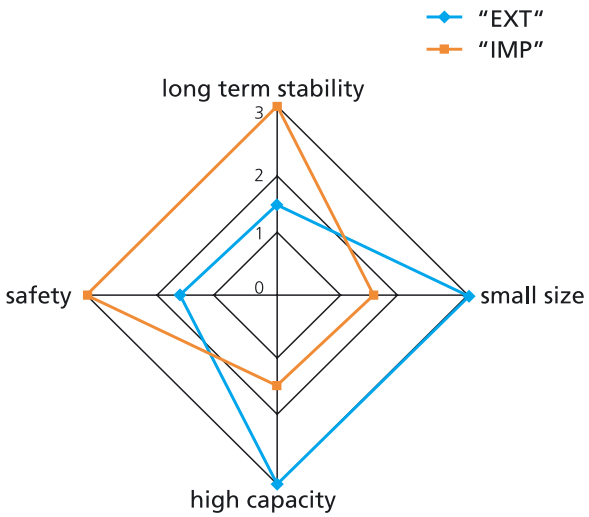


Figure 1: Focal points of rechargeable batteries for external hearing aids ("EXT") and implantable hearing aids ("IMP").

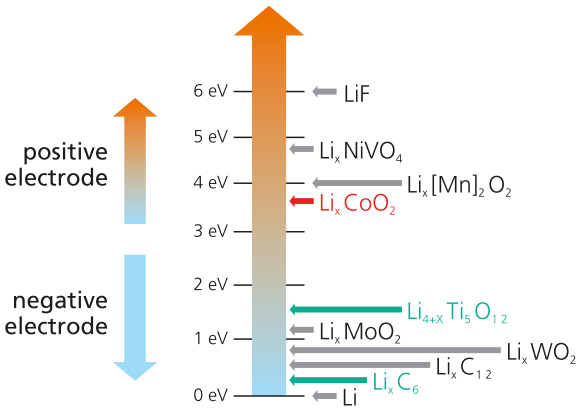


Figure 2: Electromotive series of lithium compounds (green arrows: anode materials, red arrow: cathode material).

Figure 4: View of the Ti- shell of the „IMP"- battery.

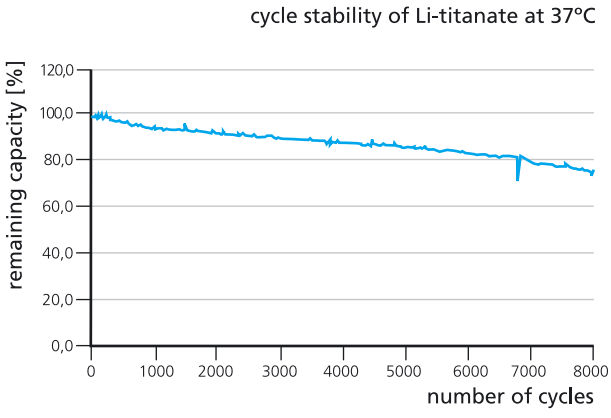


Figure 3: Cycle test of a Li-titanate cell (2,3 V, 37° C).

The "IMP" battery characteristics: For an implantable battery safety, reliability and lifetime are the most challenging aspects. E.g. a lifetime of at least 10 years is targeted. For these reasons the robust Lithium-titanate based chemistry (U = 2,3 V) has been selected.
The key experiment with regard to the electrical performance of the implantable battery is a long term test close to real life conditions. On the other hand, it has to be a compromise between project duration and the projected life time of the implantable battery. After 7300 cycles at 37 °C the Lithium-titanate battery showed a remarkably low capacity fade of about 20 %

Figure 5: Prototype of a rechargeable battery in front of an external hearing aid.

with respect to the first cycle (figure 3). In terms of practical use of hearing aids this would correspond to 20 years of use with one charge/ discharge cycle per day. There is currently no rechargeable lithium battery in the market that exhibits such outstanding cycle stability. Even cycle tests with serial connected batteries without single cell monitoring indicated that series connection of the cells does not affect severely the cycle stability. An additional feature is the improved insensitivity against abuse e.g. deep discharge.

The "IMP"-housing technology: Besides the requirements concerning the electrical performance the implantable battery – consisting of battery body and battery housing – has also to comply with the particular demands of the manufacturer of the medical device and strict regulations for implantable devices. State-of-the- art technology uses titanium or stainless steel housings, sealed by laser welding, with a hermetic feed-through for the electrical terminals. With regard to leak-tightness, optimisation of energy density and assembling a double wall housing -consisting of two electrically isolated shells – has been introduced.

The outer titanium housing (figure 4) consists of two deep-drawn half shells that are

laser-welded at the perimeter. Two double feed-throughs with special wires, glass insulator and Titanium flange, are located in the symmetry plane with the flange welded to the shells. First tests of this sophisticated housing technology showed very promising results.

External hearing aids ("EXT")

External hearing aids are usually operated by non rechargeable batteries. The small and often odd shaped volume available for the battery in combination with a typical uptime of 10 to 16 hrs per day is the main challenge for the replacement of primary cells by secondary batteries since the fill factor (fraction of the total battery volume used for charge storage) of the battery strongly decreases with size. Furthermore the lifetime of the battery should be comparable to the service life of the instrument. Rechargeable batteries presently available on the market do not meet these requirements in terms of energy density and form factor flexibility.

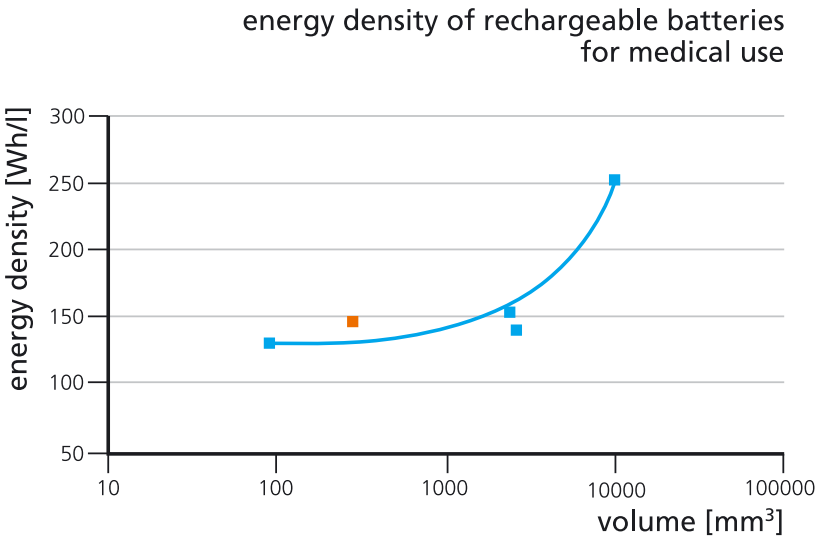


Figure 6: Energy density of commercial rechargeable batteries as a function of battery volume (orange: ISIT).

The "EXT" battery characteristics: Focal point of the development of rechargeable batteries for external hearing aids is the optimisation of the energy density. For these reasons the 3,7 V chemistry with a graphite based anode has been selected and optimised with respect to the special requirements in this application. Careful selection of electrode materials and a dedicated layout of the battery resulted in a cycle stability better than 85 % after 500 charge/discharge cycles at an energy density beyond 350 Wh/(battery body).

The battery housing for "EXT": The Li-polymer technology by itself allows for virtually all shapes of the battery body. The main challenge is the realisation of an adequate housing concept ensuring an optimised utilisation of the very limited space available in an external hearing aid (< 0,3 cm^3). The standard type housing of lithium polymer rechargeable batteries is a polymer coated aluminium foil with a surrounding sealing seam having a width of 3 to 5 mm. This is not acceptable for the use in hearing-aids. ISIT therefore decided for a polymer based housing manufactured in injection moulding technology. Despite the need for somewhat thicker walls (mechanical stability) plastic housings show some important advantages to all-metal casings:

- No danger of electrical shorts caused by the housing
- Ease of assembly
- Compatibility to battery chemistry

One example demonstrating the volume available in a "Behind-The-Ear" hearing aid (BTE) is shown in figure 5. In other applications like CIC (Completely In Channel) or ITE (In The Channel) the volume is even smaller. Even though only little information is available concerning rechargeable batteries for use in medical applications, a comparison of the latest generation of "EXT"– batteries with commercial such products – shows that the energy density of the ISIT-solution at a given volume is superior (figure 6).

Important Names, Data, Events
Annual Report 2005

Lecturing Assignments at Universities

H. Bernt:
Halbleitertechnologie I und II, Technische Fakultät der Christian-Albrechts-Universität, Kiel

A. Heuberger:
Lehrstuhl für Halbleitertechnologie, Christian-Albrechts-Universität, Kiel

Memberships in Coordination Boards and Committees

T. Ahrens:
Member of ELF NET (European Leadfree Network)

T. Ahrens:
Coordinator of AOI-Anwenderkreis (Automated Optical Inspection)

T. Ahrens:
Member of DVS Fachausschuss Löten

T. Ahrens:
Member of DVS Fachausschuss Mikroverbindungstechnik

T. Ahrens:
Member of Hamburger Lötzirkel

W. H. Brünger:
Member of Steering Committee: Electron, Ion and Photon Beams and Nanofabrication, EIPBN, USA

W. H. Brünger:
Member of VDI Fachausschuss: Maskentechnik, VDI, Düsseldorf

W. H. Brünger:
Section Head: Micro and Nano Engineering, MNE 05, Wien

A. Heuberger:
Advisory Editor of International Journal of Semiconductor Manufacturing Technology; Microelectronic Engineering

A. Heuberger:
2. Chairman of an International Conference on Micro Electro, Opto, Mechanic Systems and Components

K. Pape:
Member of VDI Fachausschuss Assembly Test, VDI, Frankfurt

K. Pape:
Member of BVS, Bonn

K. Pape:
Member of FED

M. H. Poech:
Member of „Arbeitskreis Bleifreie Verbindungstechnik in der Elektronik“

W. Reinert:
Speaker of working group „Wafer level packaging“ in ZVEI

W. Reinert
Member of Arbeitskreis A 2.4 Drahtbondtechnik, DVS

M. Reiter:
Member of Gf Korr “Arbeitskreis Korrosionsschutz in der Elektronik“

M. Reiter:
Member of “Arbeitskreis Lotpasten“

M. Reiter:
Member of “Arbeitskreis Bleifreie Verbindungstechnik in der Elektronik“

M. Reiter:
Member of “Industrie-Arbeitskreis Know-How-Transfer mikrotechnischer Produktion“

G. Zwicker:
Head of Fachgruppe Planarisierung/ Fachausschuss Verfahren/ Fachbereich Halbleitertechnologie und -fertigung der GMM des VDE/VDI

G. Zwicker:
Member of International Advisory Committee of PacRim-2005 CMP Conference

Distinctions

Ragna-Berenike Rühe
Auszeichnung der IHK-Schleswig-Holstein als Landesbeste in der Abschlussprüfung zur Mikrotechnologin (Mikrosystemtechnik), Elmshorn, September 20, 2005

Rainer Hintsche
European Grand Prix of Innovation, Preis für angewandte Forschung und Technologieentwicklung: Anwendung der elektrischen Biochiptechnologie zur Detektion von biologischen Gefahrenstoffen, Monaco, December 10, 2005

Wilhelm Brünger
Hommage at MNE for scientific work on Ion Projection Lithography, Wien, September, 2005

Cooperation with Institutes and Universities

Technical University of Budapest, Department of Electronics Technology, Hungary

Cambridge University, UK

Rutherford Appleton Laboratories, Didicot, UK

Technische Universität Dresden, Institut für Halbleiter- und Mikrosystemtechnik

VTT, Espoo, Finland

Fachhochschule Flensburg

University of Gdansk

Ernst-Moritz-Arndt-Universität (EMAU), Greifswald

CEA Leti, Grenoble, France

ESRF, Grenoble

Technion, Haifa, Israel

Universitätskrankenhaus Eppendorf, Hamburg

Fachhochschule Westküste, Heide

Technische Universität, Ilmenau

Institut für Fügetechnik und Werkstoffprüfung (IFW), Jena

Christian-Albrechts-Universität, Technische Fakultät, Kiel

Fachhochschule Kiel

MIMOS, Kuala Lumpur, Malaysia

École Polytechnique Fédérale de Lausanne, Switzerland

IMEC, Leuven, Belgium

University of Linköping, Sweden

Wehrwissenschaftliches Institut, Munster

CSEM, Neuchâtel, Switzerland

Universität Oulu, Finland

CNRS, École Polytechnique, Paris, France

Universtity of Pavia, Italy

University of Pennsylvania, USA

University of Perugia, Italy

National Inst. for NBC Protection, Pribram, Czech Republic

Royal Institute of Technology (KTH), Stockholm, Sweden

VTT, Technical Research Center of Finland, Tampere, Finland

VDI/VDE-Technologenzentrum Informationstechnik, Berlin

LAAS-CNRS, Toulouse, France

Universität Ulm

Centre d'Etude le Bouchet, Vert le Petit, France

Plant Research International, Wageningen, Netherlands

Fachhochschule Wedel

Technische Universität, Wien, Austria

Trade Fairs and Exhibitions

SMT Hybrid Packaging 2005
System Integration in Micro Electronics, Exhibition and Conference, April 19 – April 21, 2005, Nürnberg

Sensor 2005
12th International Trade Fair for Sensorics, Measuring and Testing Technologies with Concurrent Conferences, May 10 – May 12, 2005, Nürnberg

Laser 2005. World of Photonics
17th International Trade Fair and International Congress, June 13 – June 16, 2005, München

Biotechnica 05
14th International Trade Fair for Biotechnology, October 18 – October 20, 2005, Hannover

Productronica 2005
16th International Trade Fair for Electronics Production, November 15 – November 18, 2005, München

Miscellaneous Events

Aspekte moderner Siliziumtechnologie
Public lectures. Monthly presentations, ISIT, Itzehoe

Der bleifreie Lötprozess in der Fertigung elektronischer Baugruppen
Seminar: February 22 – February 24 and October 18 – October 20, 2005, ISIT, Itzehoe

ISIT Presentation in the Framework of Science Tunnel Exhibition of the Max-Planck-Gesellschaft
April 4 – July 10, 2005, Ludwigshafen, Germany and September 16 – September 17, 2005, Mirakai, National Museum of Emerging Science and Innovation Tokyo, Japan

SMT-Rework-Praktikum auch mit bleifreien Loten
Seminar: April 5 – April 7 and November 8 – November 10, 2005, ISIT, Itzehoe

Manuelles Löten von SMT-Bauelementen auch mit bleifreien Loten
Seminar: April 5 – April 7 and November 8 – November 10, 2005, ISIT, Itzehoe

14. CMP Users Meeting
April 15, 2005, Forum am Deutschen Museum, München

Visit of Federal President Horst Köhler, Minister-President of Land Schleswig-Holstein Peter Harry Carstensen and Minister of Science, Economic Affairs and Transportation of Land Schleswig-Holstein Dietrich Austermann at the winners of „Deutscher Zukunftspreis 2004".
Speakers: Dr. Rainer Hintsche (ISIT), Dr. Walter Gumbrecht (Siemens), Dr. Roland Thewes (Infineon), Prof. Claus Weyrich (Siemens), Dr. Manfred Dietrich (BMBF), Minister-President Peter Harry Carstensen and Prof. Heuberger (ISIT), May 25, 2005, ISIT, Itzehoe

Inspektion in der Baugruppenfertigung
Seminar: June 07 – June 08, 2005, ISIT, Itzehoe

Press conference „ISIT wird für 12,8 Millionen Euro modernisiert"
Speakers: Dietrich Austermann (Minister of Science, Economic Affairs and Transportation of Land Schleswig-Holstein), Dr. Ingo Hussla (IZET Innovationszentrum Itzehoe) and Prof. Anton Heuberger, June 13, 2005, ISIT, Itzehoe

ISIT Presentation in the ZDF-TV-show "Der Sommer mit Knoff Hoff" (moderation Joachim Bublath)
July 6, 2005, München

Press conference "Neue Produktionstechnologien zur Mikrosystemtechnik am Standort Itzehoe"
Speakers: Dietrich Austermann (Minister of Science, Economic Affairs and Transportation of Land Schleswig-Holstein), Dr. Peter Draheim (Silicon Manufacturing Itzehoe) and Prof. Anton Heuberger, August 19, 2005, SMI, Itzehoe

Press conference „SensorDynamics und Fraunhofer ISIT: Vertikale Systemintegration in der Mikrosensorik"
Speakers: Hubertus Christ (CEO SensorDynamics) and Prof. Anton Heuberger, September 16, 2005, ISIT, Itzehoe

VABOND-Workshop on Long-term Stability of Vacuum-Encapsulated MEMS Devices Using Eutectic Wafer Bonding
September 21, 2005, ISIT, Itzehoe

ISIT Presentation in the Framework of Straschu Technologieforum
September 29, 2005, ISIT, Itzehoe

ISIT Presentation in the Framework of VDI/VDE/IT and BMBF Exhibition "Mikrowelten – Zukunftswelten"
October 10, 2005, Freiburg

15. CMP Users Meeting
October 28, 2005, Fraunhofer IISB, Erlangen

ISIT-Presentation in the Framework of "Fraunhofer meets Continental"
In-house-exhibition, Conti-Teves, Frankfurt, November 29, 2005

Opening of the "Life Environment LEADFREE Training Line"
December 6, 2005, ISIT, Itzehoe

Journal Papers and Contributions to Conferences

T. Ahrens:
Zinn-Whisker. Bleifreies Löten, Ergebnisse aus der aktuellen Forschung, DVS-Berichte 238, p. 13 – 16, Düsseldorf, 2005

L. Bertels, W. Reinert:
UV-Laserblende für schonende Hornhautabtragung. Elektronik Industrie, 11/2005, p. 83, 2005

C. Brandstaetter, E. Haugeneder, H.-J. Doering, T. Elster, J. Heinitz, O. Fortagne, S. Eder-Kapl, G. Lammer, P. Jöchl, H. Loeschner, K. Reimer, J. Saniter, M. Talmi, R. Eberhardt, K. Kroenert:
Demonstrators – a Vital Step Forward for Projection Mask-Less Lithography (PML2). Proceedings of the 21st European Mask and Lithography Conference EMLC, January 31 – February 3, Dresden, 2005

V. Dharuman, T. Grunwald, E. Nebling, J. Albers, L. Blohm, R. Hintsche:
Label-free Impedance Detection of Oligonucleotide Hybridisation on Interdigitated Ultramicroelectrodes Using Electrochemical Redox Probes. Biosensors and Bioelectronics, 21/2005, p. 645 – 654, 2005

H. Doering, T. Elster, J. Heinitz, O. Fortagne, C. Brandstaetter, E. Haugeneder, S. Eder-Kapl, G. Lammer, H. Loeschner, K. Reimer, J. Eichholz, J. Saniter:
Proof-of-Concept Tool Development for Projection Mask-Less Lithography (PML2). Proceedings of 30th SPIE International Symposium Microlithography, ML01, February 26 – March 4, San Jose, CA, USA, 2005

R. Dudde, T. Vering, G. Piechotta, R. Hintsche:
Computer Aided Continuous Drug Infusion – Set-Up and Test of a Mobile Closed Loop System for the Continuous Automated Infusion of Insulin. IEEE Transactions on Information Technology in Biomedicine, 2005

D. Friedrich, H. Bernt, H. Hanssen, K. Kohlmann, J. Schliwinski:
Innovative Power Control in High Demand. Power Systems Design, AGS Media Group, p. 32, September, 2005

D. Friedrich:
Je dünner, desto besser. Design & Elektronik, WEKA Fachzeitschriften-Verlag, 9/2005, p. 84, September, 2005

A. Heuberger, U. Hofmann:
Lesbare Projektion auf gekrümmten Oberflächen. Laser+Photonik, 04/2005, p. 46 – 48, 2005

A. Heuberger, U. Hofmann:
Mikro-Scanner projiziert auf gekrümmte Oberflächen. Mechatronik F&M, Carl Hanser Verlag, 7/2005, p. 36, July, 2005

R. Hintsche, B. Elsholz, G. Piechotta, R. Wörl, C. G. J. Schabmüller, J. Albers, V. Dharuman, E. Nebling, A. Hanisch, L. Blohm, F. Hofmann, B. Holzapfl, A. Frey, C. Paulus, M. Schienle and R. Thewes:
Fully Electrical Microarrays, in Electrochemistry of Nucleic Acids and Proteins. Towards Electrochemical Sensors for Genomics and Proteomics, Editors: E. Palecek, F. Scheller and J. Wang, Elsevier, Amsterdam, 2005

U. Hofmann:
Kleine Spiegel – große Bilder. Elektronik und Entwicklung, publish-industry Verlag, p. 22, December, 2005

M. Kröll, W. Lortz, R. Brandes, E. Stachowiak, M. Torkler, G. Zwicker:
Influences on the Polishing Results in STI and ILD CMP Using Nanostructured Fumed Ceria. Proceedings PacRim-CMP 2005, Seoul, 2005

P. Lange, B. Ohlsen, S. Puls, J. Syre:
Characterization of Ti/TiN and TiN Conductive Layer for High Temperature MEMS Devices. Mat. Res. Soc. Proc., Vol. 872, p. 57, San Francisco, 2005

P. Lange, B. Ohlsen, S. Puls, J. Syre:
High Temperature Stability of Ti/TiN and TiN Heaters on Bulk Micromachined Membranes. Sensor 2005, Proceedings I, p. 493, May 10 – May 12, Nürnberg, 2005

P. Lange:
Hohe Lebensdauer durch geringe Widerstandsdrift. Markt & Technik, WEKA Fachzeitschriften Verlag, 43/2005, p. 24, October, 2005

P. Lange:
Mikromechanischer Luftmassensensor. Sensor Report, Verlag Coating Thomas & Co., 05/2005, p. 27, October, 2005

T. Lisec, B. Wagner:
Integration Aspects of RF MEMS Technologies. Proceedings 35th European Microwave Conference 2005, Paris, 2005

T. Lisec, C. Huth, B. Wagner:
Surface Micromachined Capacitive RF Switches and Varactors. Mikrosystemtechnik Kongress 2005, p. 98, Freiburg, 2005

M. Los, J.M. Los, L. Blohm, E. Spillner, T. Grunwald, J. Albers, R. Hintsche, G. Wegrzyn:
Rapid Detection of Viruses Using Electrical Biochips and Anti-Virion Sera. Letters in Applied Microbiology 2005, 40/2005, p. 479 – 485, 2005

P. Merz, W. Reinert, K. Reimer, B. Wagner:
PSM-X2: Polysilicon Surface Micromachining Process Platform for Vacuum-Packaged Sensors. Proceedings of Mikrosystemtechnik Kongress 2005, p. 467, Freiburg, 2005

G. Piechotta, J. Albers, R. Hintsche:
Novel Micromachined Silicon Sensor for Continuous Glucose Monitoring. Biosensors and Bioelectronics, 21/2005, p. 802–808, 2005

M. H. Poech:
Thermomechanik der Baugruppe. Bleifreies Löten, Ergebnisse aus der aktuellen Forschung, DVS-Berichte 238, p. 27 – 34, Düsseldorf, 2005

J. Pontow, W. Reinert:
A Hundred Thousand Solder Balls. Elektronik Praxis, Vogel Verlag, p. 12, November, 2005

J. Pontow, W. Reinert:
100.000 Lotkugeln auf einem Wafer. EPP – Elektronik Produktion & Prüftechnik, Konradin Verlag, p. 52, October, 2005

J. Pontow, W. Reinert, K. Pape:
Wafer Level-Chip Size Packaging im industriellen Maßstab. Plus-VTE Produktion von Leiterplatten und Systemen, Eugen G. Leuze Verlag, p. 1836, October, 2005

J. Quenzer, G. Günther, H. Murrenhoff:
Ein thermisch angetriebenes, schnelles pneumatisches 2/2 Wege Ventil. Proceedings of Mikrosystemtechnik Kongress 2005, p. 705, Freiburg, 2005

K. Reimer, M. Witt, D. Kähler, J. Eichholz, L. Ratzmann, W. Brünger, H.-J. Döring, E. Haugenerder, S. Eder-Kapl, R. Nowak:
Mask Manufacture for Projection Mask-Less Lithography (PML2) – MEMS-Technology for a Programmable Aperture Plate system. Proceedings of the 21st European Mask and Lithography Conference EMLC, January 31 – February 3, Dresden, 2005

W. Reinert:
High Vacuum Wafer Bonding Technology, AuSi Eutectic Wafer Bonding with Integrated Getter Thin Film for Long Term Stable High Vacuum. MST News, Spezialausgabe über Wafer Bond Technologie, February, 2005

M. Witt, J. Eichholz, L. Ratzmann, D. Kähler, W. Brünger, K. Reimer, H.-J. Döring, E.Haugenerder:
Development of Microsystem Technologies for a Monolithically Integrated Programmable Aperture Plates System used in Mask Less 45 nm e-Beam Lithography Tools. Proceedings of Mikrosystemtechnik Kongress 2005, October 10 – October 12, Freiburg, 2005

G. Zwicker:
A Comparison of CMP Requirements for Microelectronics and MEMS Manufacturing. Proceedings PacRim-CMP 2005, Seoul, 2005

X. Xie, Z. Berner, J. Albers, D. Stüben:
Electrochemical Behavior and Analytical Performance of an Iridium-Based Ultramicroelectrode Array (UMEA) Sensor. Microchim Acta 150, p. 137–145, 2005

Talks and Poster Presentations

T. Ahrens:
Lead-Free Wave Soldering with Various Solder Alloys. Cobar Benelux-Seminar, Breda, January 27 – January 28, 2005

T. Ahrens:
Lötqualität. Seminar: Der bleifreie Lötprozess in der Fertigung elektronischer Baugruppen, ISIT, Itzehoe, February 22 and October 18, 2005

T. Ahrens:
Baugruppen- und Fehlerbewertung. Seminar: Der bleifreie Lötprozess in der Fertigung elektronischer Baugruppen, ISIT, Itzehoe, February 23 and October 19, 2005

T. Ahrens:
Fertigungsgerechtes Design. Seminar: Der bleifreie Lötprozess in der Fertigung elektronischer Baugruppen, ISIT, Itzehoe, February 24, 2005

T. Ahrens:
Was wird anders durch bleifreies Löten. Seminar: Der bleifreie Lötprozess in der Fertigung elektronischer Baugruppen, ISIT, Itzehoe, February 24 and October 20, 2005

T. Ahrens:
Bleifreies Handlöten. 8. Europäisches Elektroniktechnologie-Kolleg, Colonia de Sant Jordi, Mallorca, March 12, 2005

T. Ahrens:
Bleifrei Reparaturlöten. Seminar: Manuelles Löten von SMT-Bauelementen auch mit bleifreien Loten, ISIT, Itzehoe, April 5 and November 8, 2005

T. Ahrens:
Leadfree Soldering in the Semiconductor Industry. Creating Baltic Business – Technology Forum & Matchmaking, IZET, Itzehoe, April 21, 2005

T. Ahrens:
Design-Review für die Bleifrei-Umstellung. Straschu Industrie-Elektronik Workshop: RoHS-konforme Baugruppenfertigung, Stuhr, May 3, 2005

T. Ahrens:
Forum und Minimesse als wertfreie und konzentrierte Informationsvermittlung. Seminar: Inspektion in der Baugruppenfertigung, ISIT, Itzehoe, June 7, 2005

T. Ahrens:
Inspektion bleifreier Lötstellen. Seminar: Inspektion in der Baugruppenfertigung, ISIT, Itzehoe, June 7, 2005

T. Ahrens:
AOI/AXI-Inspektion RoHS-konformer bleifreier Lötstellen – Methodik, Einsatzbereich, Verbreitung. 13. FED-Konferenz, Elektronik-Design – Leiterplatten – Baugruppen 2005, Fulda, September 24, 2005

T. Ahrens:
Fertigungsgerechtes Design. Straschu Technologieforum 2005, ISIT, Itzehoe, September 29, 2005

T. Ahrens:
Fakten zu RoHS. Farnell inOne RoHS Info Tag, Hamburg, October 5, 2005

T. Ahrens:
Sn-Whisker – Wissenschaftlicher Hintergrund und Prüfverfahren, Düsseldorf, October 6, 2005

T. Ahrens:
Gesetzeslage RoHS, Anforderungen an zukünftige Elektronikproduktion, Rahmenbedingungen, Konsequenzen hinsichtlich technologischer Prozesse, Design-Rules. 32. Stammtisch Mikroelektronik und Mikrosystemtechnik, Hamburg, November 1, 2005

T. Ahrens:
Was ist „RoHS"? – und was geht mich das an?, Open House 2005 der SEF Roboter GmbH, Scharnebeck, November 8, 2005

T. Ahrens, A. Hussla, C. Herrmann:
Projekt und Konzept der "bleifrei-Trainingslinie"; grüne Elektronik durch Life Cycle Assessment. Seminar: Life Environment LEADFREE Training Line, ISIT, Itzehoe, December 6, 2005

W. Brünger, A. H. Dietzel, H. Löschner:
Ion Projection Surface Structuring with Noble Gas Ions at 75 KEV. 14th Inernational Conference on Surface Modification of Materials by Ions Beams, KuSadasi, Turkey, September 4 – September 9, 2005

S. Eder-Kapl, E. Haugeneder, H. Langfischer, K. Reimer, J. Eichholz, M. Witt, H.-J. Doering, J. Heinitz, C. Brandstaetter:
Projection Mask Less Lithography (PML2): First results from the Multi Beam Blanking Demontrator, MNE, Wien, September, 2005

J. Eichholz:
Microsensors and Actuators for Ambient Intelligence Applications. MIMOSA Workshop: Invisible Electronics for Ambient Intelligence Applications, Grenoble, September 16, 2005

B. Elsholz, R. Wörl, J. Albers, L. Blohm, H. Feucht, R. Hintsche:
Automatisierte elektrochemische Detektion von bakterieller 16S rRNA auf Low-Density Mikroarrays. Regensburg, March 13 – March 15, 2005

P. Gulde:
Entwicklung maßgeschneiderter LiPo-Akkus für medizinische und andere Anwendungen. Seminar: Aspekte moderner Siliziumtechnologie, ISIT, Itzehoe, November 2, 2005

R. Hintsche:
Electrical Biochip Technology. Creating Baltic Business – Technology Forum & Matchmaking, IZET, Itzehoe, April 21, 2005

M. Kröll, R. Brandes, W. Lortz, E. Stachowiak, M. Torkler, G. Zwicker:
Fumed Ceria for Use in STI and ILD CMP. 14. CMP Users Meeting, München, April 15, 2005

M. Kröll, W. Lortz, R. Brandes, E. Hübscher, M. Torkler, G. Zwicker:
Influences on the Polishing Results in STI and ILD CMO Using Nanostructured Fumed Ceria. PacRim-CMP 2005, Seoul, South Korea, November 17 – November 19, 2005

P. Lange, B. Ohlsen, S. Puls, J. Syre:
Characterization of Ti/TiN Conductive Layer for High Temperature MEMS Devices. MRS Spring Meeting 2005, San Francisco, March 28 – April 1, 2005

P. Lange, B. Ohlsen, S. Puls, J. Syre:
High Temperature Stability of Ti/TiN and TiN Heaters on Bulk Micromachined Membranes. Sensor 2005, Nürnberg, May 10 – May 12, 2005

O. Lawin:
AOI Kalibrierprobe. Seminar: Inspektion in der Baugruppenfertigung, ISIT, Itzehoe, June 8, 2005

G. Longoni, M. Amiotti, A. Conte, M. Moraja, W. Reinert:
Q-factor Enhancement for MEMS Devices by the Getter Film at Wafer Level. Micro System Technologies 2005, Munich, 2005

P. Merz, W. Reinert, K. Reimer, B. Wagner:
PSM-X2: Polysilicon Surface Micromechanic Process Platform for Vacuum Package Sensors. Mikrosystemtechnik Kongress 2005, Freiburg, October 10 – October 12, 2005

P. Merz:
PSM-X2: Silizium-Oberflächenmikromechanischer Prozess zur Herstellung von vakuumverpackten Inertialsensoren für die Automobilindustrie. Vortragsreihe VDE Region Nord e. V., Helmut-Schmidt-Universität, Universität der Bundeswehr Hamburg, Hamburg, November 30, 2005

E. Nebling, A. Hanisch, J. Albers, L. Blohm, S. Deckers, R. Hintsche:
Nachweis von Antibiotikarückständen in Milch mittels elektrischer Biochiptechnologie. 4. Deutsches BioSensor Symposium, Regensburg, March 13 – March 16, 2005

G. Neumann:
Maßgeschneiderte Akkus in Lithium-Polymer-Technologie. In-house-exhibition "Fraunhofer meets Continental", Frankfurt, November 29, 2005

Scientific Publications

G. Piechotta, J. Albers, L. Blohm, R. Hintsche:
Automatisierter elektrochemischer Nachweis von Toxinen auf Biosensoren. Biosensor-Kongress 05, Regensburg, March 15, 2005

M. H. Poech, W. Graf, A. Greif:
Power Cycling of Discrete TO220 MOSFETs. ECPE Workshop „Building in Reliability into Power Electronic Systems", Nuremberg, January 13 – January 14, 2005

M. H. Poech:
Das Reflow-Lötprofil. Seminar: Der bleifreie Lötprozess in der Fertigung elektronischer Baugruppen, ISIT, Itzehoe, Feb. 22 and Oct.18, 2005

M. H. Poech:
Zuverlässigkeit von Lötstellen. Seminar: Der bleifreie Lötprozess in der Fertigung elektronischer Baugruppen, ISIT, Itzehoe, February 24 and October 19, 2005

M. H. Poech:
Thermomechanik der Baugruppe. 2. Kolloquium „Bleifreies Löten", DVS, Düsseldorf, October 6, 2005

M. H. Poech:
Bleifreies Handlöten. OTTI Seminar „Weichlöten – die wichtigste Verbindungstechnologie in der Elektronik", Würzburg, October 18 – October 19, 2005

J. Pontow:
Chip-Size-Packaging im industriellen Maßstab. Seminar: Aspekte moderner Siliziumtechnologie, ISIT, Itzehoe, June 1, 2005

K. Reimer:
Mask Manufacture for Projection Mask-Less Lithography (PML2) – MEMS-Technology for a Programmable Aperture Platesystem. The 21st European Mask and Lithography Conference EMLC, Dresden, January 31 – February 3, 2005

K. Reimer:
Programmierbares Ablenksystem für die maskenlose Elektronenstrahllithographie im Nanometerbereich. Seminar: Aspekte moderner Siliziumtechnologie, ISIT, Itzehoe, October 5, 2005

W. Reinert:
Vacuum Wafer Bonding Technology. MicroTech 2005, Cambridge, March, 2005

W. Reinert, D. Kähler, M. Oldsen, P. Merz:
In-line Critical Leak Rate Testing of Vacuum-Sealed and Backfilled Resonating MEMS Devices. Proceedings of the 207th Electochemical Society Meeting, Quebec City, Canada, May, 2005

W. Reinert:
Hermeticity Test to Predict the Vacuum Lifetime in Individual Micro- and Nano-Liter Packages. VABOND-Workshop on Long-term Stability of Vacuum-Encapsulated MEMS Devices Using Eutectic Wafer Bonding, Itzehoe, September 21, 2005

W. Reinert:
Vakuumdichte Gehäuse für hochempfindliche mikromechanische Sensoren. Seminar: Aspekte moderner Siliziumtechnologie, ISIT, Itzehoe, September 7, 2005

W. Reinert, D. Kähler:
Assessement of Vacuum Lifetime in nL-Packages. EPTC 2005, Singapore, December, 2005

M. Reiter:
Bewertung bleifreier Lötverbindungen. Technologie-Seminar, Siebtronic, Salzburg, April 13, 2005

M. Reiter:
Oberflächenbewertung elektronischer Baugruppen. Workshop: Oberflächenqualifikation für elektronische Baugruppen, Ingolstadt, June 16, 2005

M. Reiter:
Kontamination und Korrosion elektrischer Baugruppen. Technologietag, Salzburg, October 5, 2005

M. Reiter:
Kontamination und Korrosion elektrischer Baugruppen. Workshop: Oberflächenqualifikation für elektronische Baugruppen, Ingolstadt, December 1, 2005

C. Schabmueller, G. Piechotta, D. Loppow, B. Schütze, J. Albers, R. Hintsche:
Siliziumsensor zur Laktatmessung im Speichel. Regensburg, March 13 – March 15, 2005

H. Schimanski:
Qualitätsfaktor Leiterplatten. Seminar: Der bleifreie Lötprozess in der Fertigung elektronischer Baugruppen, ISIT, Itzehoe, February 23 and October 19, 2005

H. Schimanski:
CSP-Underfill. Seminar: Der bleifreie Lötprozess in der Fertigung elektronischer Baugruppen, ISIT, Itzehoe, February 24 and October 20, 2005

H. Schimanski:
Reparatur komplexer SMT-Baugruppen. Seminar: Manuelles Löten von SMT-Bauelementen, ISIT, Itzehoe, April 5 and November 8, 2005

H. Schimanski:
Rework-Strategien für bleifreies Löten – Sichere Prozessführung durch Optimierung und Festlegung der Arbeitsschritte. OTTI Seminar „Produktion bleifreier elektronischer Baugruppen", Würzburg, June 14, 2005

H. Schimanski:
Rework bleifreier elektronischer Baugruppen. 13. FED-Konferenz, Elektronik-Design – Leiterplatten – Baugruppen 2005, Fulda, September 24, 2005

O. Schwarzelbach:
Entwicklung von Drehratensensoren für die Automobilindustrie. Seminar: Aspekte moderner Siliziumtechnologie, ISIT, Itzehoe, May 4, 2005

B. Wagner:
MOEMS – Miniaturization of Optical Microsystems. Syddansk Universitet, Sønderborg, November 24, 2005

M. Witt:
Entwicklung der MEMS-Technologie für ein programmierbares Apertur Platten System zur Verwendung in maskenlosen 45 nm e-Beam Lithographiegeräten. Mikrosystemtechnik Kongress 2005, Freiburg, October 10 – October 12, 2005

R. Wörl:
Fortschritte in der Nukleinsäureanalytik mit elektrischen Biochips. Seminar: Aspekte moderner Siliziumtechnologie, ISIT, Itzehoe, April 6, 2005

R. Wörl, R. Hintsche:
Vor Ort Analytik biologischer Kampf- und Schadstoffe. Biosensor-Kongress 05, Regensburg, March 14, 2005

S. Zerbini, A. Fourier, W. Reinert:
Three Industrial Sample Applications of Successful Getter Integration. VABOND-Workshop on Long-term stability of Vacuum-Encapsulated MEMS Devices Using Eutectic Wafer Bonding, Itzehoe, September, 2005

G. Zwicker:
Chemisch-mechanisches Polieren von MEMS-Bauelementen. Freiberger Siliziumtage 2005, Freiberg, June 17, 2005

G. Zwicker, E. Hübscher, M. Torkler, M. Zellmer, G. Hey:
Untersuchung zum Polierverfahren einer Levasil 50CK30 colloidal-silica Slurry. 15. CMP Users Meeting, Erlangen, October 28, 2005

G. Zwicker:
A Comparison of CMP Requirements for Microelectronics and MEMS Manufacturing. PacRim-CMP 2005, Seoul, South Korea, November 17 – November 19, 2005

G. Zwicker:
Application of Chemical-Mechanical Polishing (CMP) for the Manufacturing of MEMS Devices. REED Technical Seminar: „Leading Edge MEMS Manufacturing Processes", Tokyo, Japan, November 28, 2005

G. Zwicker:
Chemisch-mechanisches Polieren (CMP) für die Herstellung von MEMS-Bauelementen. Industriearbeitskreis-Treffen zum Projekt FINO, FH-München, December 8, 2005

Doctoral Theses

M. Shakray:
Design and Investigation of Microelectromechanical (MEMS) Varactors.
Christian-Albrechts-Universität Kiel, Technische Fakultät, May, 2005

Diploma Theses

J. Bause:
Entwicklung einer Ansteuerungs-elektronik für einen Vibrations-prüfstand.
Fachhochschule Wedel, September, 2005

P. Blicharski:
Aufbau und Programmierung einer Ansteuer-Elektronik für ein miniaturisiertes scannendes Laser-Projektions-Display.
Fachhochschule Wedel, February, 2005

S. Bölke:
Entwicklung eines automatisierten Nachweises für Botulinus Toxin auf elektrischen Biochips.
Fachhochschule Flensburg, September, 2005

T. Haartje:
Vergleich ausgewählter Vakuum-Waferbond-Technologien zur Verkappung von resonanten Mikrosensoren.
Fachhochschule Wedel, February, 2005

M. Heller:
Entwurf und Simulation eines Sensors zur Messung von Drehgeschwindigkeiten in der Z-Ebene.
Fachhochschule Kaiserslautern, February, 2005

L. Kamp:
Integration einer Onchip-Iridium-Iridiumoxid-Referenzelektrode auf einen elektrischen Biochip mit anschließender Funktionsprüfung.
Fachhochschule Kaiserslautern/Zweibrücken, March, 2005

F. Rodenwald:
Evaluierung von Ceroxid Slurries.
Fachhochschule Wedel, March, 2005

R. Zhang:
System and Process Characterization of Rework Soldering System.
Technische Fakultät der Christian-Albrechts Universität zu Kiel, February, 2005

Overview of Projects

- Prozesse/ Verfahren für die Herstellung ultradünner Trench-IGBTs auf sub-100µm Silizium-Substraten
- Entwicklung einer UBM/BCB Technologie für Wafer Level Packaging
- Fabrication of Si-Microstructures based on SOI-Wafers
- Prozessentwicklung und Unterstützung bei der Produktion von Philips-Wafern
- Fabrication of Capacitor Structures
- Entwicklung von Platinwiderständen auf Keramiksubstraten
- Carbon Nanotube Devices, CANDICE
- Bleifreie Galvanik
- Durchkontaktierung von Leistungsbauelementen
- Super Junction PowerMos
- Microtriode
- Entwicklung eines Silizium-Trenchätzprozesses mit hohen Aspektverhältnissen
- Entwicklung von Post-CMP-Reinigungsprozessen für die Fertigung von zukünftigen integrierten Schaltkreisen in der Si-Technologie
- Evaluierung von Slurries zum chemisch-mechanischen Polieren von SiO_2
- Untersuchung der Polier-eigenschaften verschiedener TiO_2-Dispersionen für Oxid-CMP (STI) und mono-Si-CMP
- Untersuchung von Ceroxid-Dispersionen für CMP

- Untersuchung an mikromecha-nischen Drehraten-Sensoren
- Entwicklung von kapazitiven HF-Schaltern
- Entwicklung von piezo-elektrischen Schichten für Si-Mikroaktuatoren
- Herstellung mikrooptischer Linsenarrays aus Glas
- Entwicklung eines Wasserstoffsensors
- Microsystems Platform for Mobile Service and Applications – MIMOSA
- AMICOM: Advanced MEMS for RF and Millimeter Wave Communications, Network of Excellence
- PML2, Projection Maskless Lithography; Development of an Aperture Plate System
- Entwicklung von Messstrategien zur Evaluierung von Parametern für MEMS Design
- Mikroscann-Systeme für Display Anwendungen
- Mikrotechnische Fabrikation von Laserresonator Spiegeln
- Charged Particle Nanotech, CHARPAN
- Radical Innovation Maskless Nanolithography, RIMANA
- Mikrosystemtechnische Laserprojektion zur informatori-schen Fahrerassistenz, MICLAS
- Studie zu Siliziummikrofonen
- Study on Silicon MEMS Force Sensors, SMErobot

- Customer Support and Design Centre for Physical Measurement Systems, EUROPRACTICE CCMeSys
- Microactuator Competence Centre, EUROPRACTICE CCMicro

- Electric DNA Chips for Bioprocess Control
- Innovative Measures for Protection against CBRN Terrorism, IMPACT
- Electrical Bio Sensor Arrays for Analyses of Harmful Micro Organisms and Microbial Toxins, eBiosense
- Genotype-Specific Hepatitis C Diagnostic Chip, HCV

- Chipkartenbestückung mit Grautonblenden
- Ultra-Thin Packaging Solutions using Thin Silicon
- Flip Chip Die Bonder for Ultra-Thin Silicon
- Stressoptimierte Montage und Gehäusetechnik für mikromechanisch hergestellte Silizium-Drehratensensoren
- Ag Thick Film Bumping on Wafer Level
- Thin Wafer Handling for Backsite Processing
- Volumeneffekte und technische Zuverlässigkeit von bleifreien Lötstellen
- Oberflächeneffekte von Komponenten zum bleifreien Löten
- Glassfritt Vacuum Wafer Bonding
- Glaslotbonden mit strukturierten Capwafern und Musterwafern
- Bewertung von Aufbaukonzepten für ein Leistungsmodul
- Assembly Test on PCB
- Qualitätsbewertung an bleifreien Baugruppen
- Automotives Mikrokamerasystem für Fahrzeugumfelderfassung, µ-CAM
- Downscaled Assembly of Vertically Interconnected Devices, DAVID
- Pan-Mobile Erfassung mit optimierten Smart-Labels zur Effizienzsteigerung von Logistikprozessen, PESEL
- Demonstration and Training Lead-Free Soldering for European Industrie, LIFE
- Wafer Level Packaging
- Wafer Level Balling for 100 µm up to 500 µm Spheares

- Hearing – Aids with Rechargeable Power Supply, HARPOS

Patents

J. Janes, U. Hofmann
Vorrichtung zum konfokalen optischen Abtasten eines Objekts
DE 103 59 853 B3

R. Bredehorst, R. Hintsche, R. Seitz, W. Gumbrecht
Method for Producing Detection Systems with Planar Arrays
US 6,881,379 B1

H. J. Quenzer, A. V. Schulz, B. Wagner, P. Merz
Verfahren zur Strukturierung eines aus glasartigem Material bestehenden Flächensubstrats
EP 1 371 092 B1

H. J. Quenzer, P. Merz, A. V. Schulz
Verfahren zur Strukturierung von Oberflächen von mikromechanischen und/oder mikrooptischen Bauelementen und/oder Funktionselementen aus glasartigen Materialien
DE 199 56 654 B4

P. Birke, G. Neumann
Verfahren zum Herstellen selbsttragender oder auf einem Substrat aufliegender, in elektrochemischen Bauelementen verwendbarer Schichten und Zwischenprodukte hierfür
DE 199 64 159 B4

L. Lisec
Vorrichtung zum Pipettieren einer Flüssigkeit
DE 101 35 963 B4

H. J. Quenzer, P. Merz, A. V. Schulz
Method for producing micromechanical and micro-optic components consisting of glass-type materials
US 6,951,119 B1

J. Eichholz
Steuerschaltung zum Steuern einer Elektronenemissionsvorrichtung
EP 1 522 211 B1

R. Bredehorst, R. Hintsche
Verfahren zum Herstellen von Detektionssystemen mit planaren Arrays
EP 1 171 768 B1

R. Sittig, D. Nagel, R. Dudde, B. Wagner, K. Reimer
Termination of semiconductor components
US 6,956,249 B2